A 3-Bit Pseudo Flash ADC Based Low-Power CMOS Interface Circuit Design for Optical Sensor

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The paper presents a CMOS interface circuit design for optical pH measurement that can produce an 8-bit digital output representing the color information (i.e., wavelength, l). In this work we are focusing at reducing the component count by design and hence reducing the cost and silicon area. While it could be further optimized for lower power consumption, the proposed design has been implemented using standard cells provided by the foundry (i.e., AMS 0.35 μm CMOS) for proof of concept. The biasing current and power consumption of the fabricated chip are measured at 11 μA and 37 μW respectively using 3.3 V supply voltage. Experimental results have further validated the proposed design concept. The number of detectable colors is eight and can be extended to a higher number without any major change in the architecture.

Keywords: CMOS, Interface Circuit, Optical Sensor, Low Power.

1. INTRODUCTION

Low cost and low power sensing is becoming a very important feature in emerging microsystems applications particularly in the area of biomedical and minimally invasive medical devices. Optical sensors are used in (bio) chemical,[1–3] monitoring biological events[4–6] and environmental sensing applications such as level measurement for pH O$_2$, CO2, and determination of molecular concentration.[7–9,23,24] Optical sensors are of primary interest to the research community due to their intrinsic advantages such as suitability for in-line measurement, low cost and long term usage. Moreover, optical pH sensors, for instance, (Photometric sensors) are non-intrusive (i.e., they don't require direct contact with the analyte); not affected by electrical or electromagnetic interferences and more suited to applications requiring sterilization.[9–12]

In addition to sensing, interface circuitry is typically required in order to perform signal conditioning and more importantly equip the system with smarter features and functionalities while reducing cost, power and system physical volume. This paper presents the design of an ultra-low power interface circuit for a portable, smart optical sensor enabling single chip implementation with reduced power consumption. The interface circuit

proposed in this paper can be used for optical pH measurement.

2. WORKING PRINCIPLE

Optical pH sensors analyze the color change produced when an indicator dye is added to a solution under test (SUT) and determine the pH level. Indicator dyes are weak acids or bases that form equilibrium in a solution as shown in (1).[13, 14] The color change of the solution depends on the relative proportion of the acid-base form of the indicator; and this proportion depends on the hydrogen level (H$^+$) which in turn represents the pH level of the solution.

$$\text{Dye}^Z(\text{acid}) + \text{H}^+ \overset{Ka}{\Longleftrightarrow} \text{HDye}^{Z+1}(\text{base}) \qquad (1)$$

Measurement of pH with the proposed microsystem can be carried out with the setup as shown in Figure 1. A white light generated from a light source will be coded by the color of the solution as it passes through it, and the light wavelength will be processed by the light sensor microsystem to determine the pH level. Similar methods have been used previously.[8]

A complete optical sensor microsystem consists of a light transducer, a preamplifier circuit and an interface circuit. The light traducer is necessary to interface the external world to the electrical circuit. It converts the incident light signal falling on its active part into an electrical
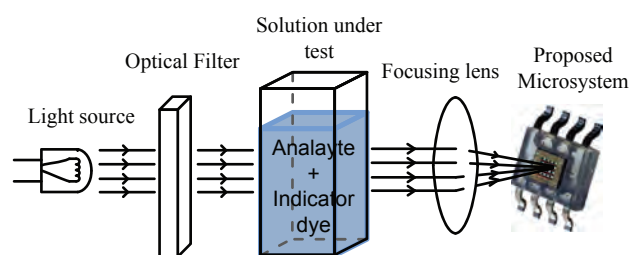

Fig. 1. Proposed pH measuring setup using the smart optical sensor.

signal (i.e., photocurrent). There are many types of light transducers available for use.[15, 16] In this work, monotony of the light transducer used is important to achieve the desired interval mapping of the voltage levels to their digital value. An OPT301 photodiode from Burr Brown[17] is selected as a photodetector. Its response in the visible region (400 nm–780 nm) is fairly monotonic as can be illustrated in Figure 2.

A dedicated interface circuit for optical sensor application is presented in this paper. Figure 3 illustrates the working principle of the proposed interface circuit as opposed to the conventional architecture of a typical optical sensor. Typical optical sensor consists of:
(i) a sensing element responsible for converting the detected light to an electrical signal;
(ii) an interface block to pre-amplify the signal and/or change the signal from current to voltage domain;
(iii) an ADC to convert the analog input to digital output for a fully digital processing;
(iv) a DSP for further signal processing which may include a memory, digital comparator arrays, arithmetic units and so on depending on the application at hand.

The interface circuit introduced in this paper reads an analog input from a transducer and outputs a digital value corresponding to the detected light. The proposed system, shown in Figure 3(b), uses an interface circuit which

consists of two comparators, two multiplexers and a few logic gates and does not require the use of further signal processing components.

The interface circuit based on a conventional flash ADC is analogous in design but features some valuable key points:
(i) The proposed interface circuit requires only two comparators regardless of the number of colors (number of output bits) being detected as opposed to conventional flash ADC which has 2^N-1 comparators, where N is the number of converted digital output bits. By minimizing the number of comparators, the power consumption can be greatly reduced as well as the on-chip area with some trade-off with the speed of conversion.
(ii) The proposed design uses tunable resistors to store analog memory that represents the light transducer response. Hence the proposed interface circuit serves the purpose of analog-to-digital conversion as well as outputting the final color information in digital form by comparing with the pre-stored color values (color representing voltage).
(iii) The interface circuit uses simple LEDs to display the output. LEDs draw considerable power from the interface circuit, for such reason, the output bits in the interface circuit are decoded to be only one bit "hot" ("1") at a time representing the corresponding color. Moreover, the duration of the active bit (duty cycle) is controlled by the optional timer included in the design. Such efforts are done towards further reducing power consumption of the overall system during implementation. Figure 4 illustrates comparison of a typical flash ADC and the proposed interface circuit design graphically.

3. DESIGN
The proposed interface circuit, shown in Figure 5, is a mixed signal solution containing both analog and digital
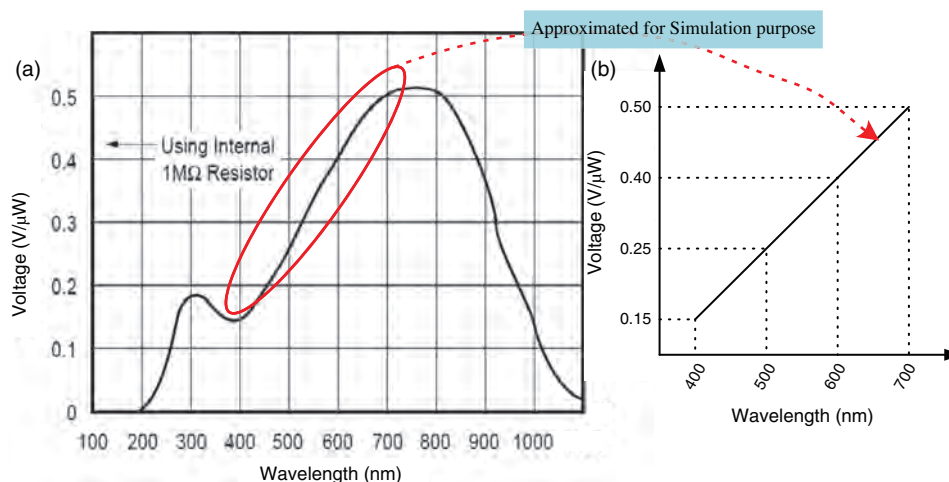

Fig. 2. (a) OPT301 photodiode response,[17] (b) approximated as a linear region for simulation purpose.

(a) Conventional optical sensor system

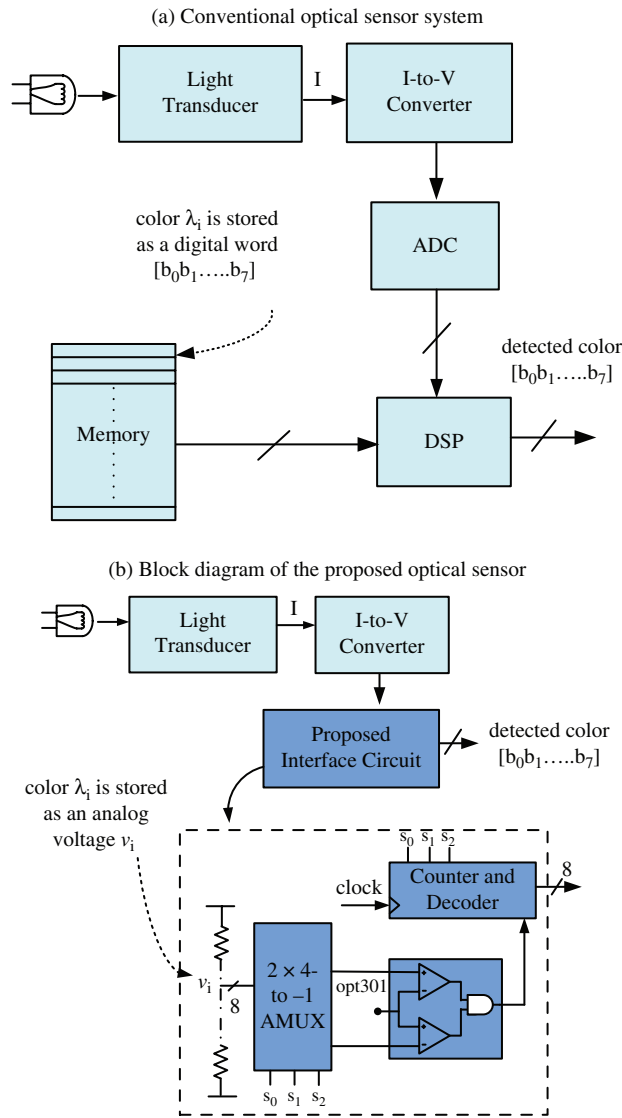(b) Block diagram of the proposed optical sensor

Fig. 3. Block diagram of (a) Conventional optical sensor system (Fully Digital processing) and (b) Block diagram of the proposed optical sensor (mixed-signal solution).

blocks. The design includes the following building blocks: a resistor ladder, analog multiplexers, comparators, a decoder and an optional timer.[18, 22, 25] It accepts analog input voltages from the optical transducer and produces 8-bit digital words that represent the incident light (i.e., λ) color with the help of pre-calibrated storage elements.

The resistor network stores predefined voltage levels such that each interval corresponds to a particular color value (in voltage). These voltages can be tuned to represent the light transducers' response when exposed to specific wavelength light and normalized with the incident power. Two 8-to-1 analog multiplexers (AMUX1 and AMUX2) are used to select the reference voltages for comparison with the optical transducer voltage. The comparators used in the design are taken from the AMS library. They draw a current of 5.28 μA at 3.3 V which shows they consume

more than 90% of the total power consumption. For future implementation, a customized comparator will be used instead to further reduce the power consumption.

The operating principle of the proposed design is shown by the Figure 6. The multiplexers switch through the reference voltages. Two multiplexers are required so that at any time two consecutive reference voltages are selected for comparison creating a closed interval. Then the transducer output is compared using comparators to decide in which interval the value falls. Both comparators go high simultaneously when the searching AMUXs enclose the right interval containing the transducer output as can be seen in Figure 6(b). At this point, the signal from AND activates the decoder and the counter state is decoded to show in which interval the color response is found. The design on this block will be discussed shortly.

3.1. Timer (Optional Block)

A timer block is an optional block added to control the duration of the active bits in the output and hence the power drawn by the display unit (LEDs). A non-retriggerable timer shown in Figure 7 is proposed and used as the timer block. The D input is tied to a digital high value ("1") and the enable input is controlled by the signal issued from the AND'ing of the signals issued from the comparators output when a particular color interval is detected, which is the signal enabling the decoder and whose duration needs to be controlled. Initially, Q value is assumed to be low and hence the PMOS transistor is turned ON resulting in the capacitor C_{ext} to be tied to Vdd (supply voltage) and hence getting fully charged. The signal at CLR will become low via the inverter maintaining the low value of Q which asserts our initial assumption. When a rising edge at the enable input is encountered, Q goes high, NMOS transistor turns ON and PMOS transistor turns OFF. This will discharge the capacitor through the resistor R_{ext} until it reaches the lower switching level of the Schmitt trigger which then clears the Q signal. Meanwhile the output signal (i.e., Q signal) is high for a period of time τ defined by the discharging process of the capacitor and other incoming signals through the enable will be neglected.

$$\tau = k * C_{ext} * (R_{ext} + r_{ON}) \qquad (2)$$

τ is programmable solely via the externally attached R_{ext} and C_{ext}. Whenever a triggering signal through the enable appears, the one-shot holds the signal for time τ. The mathematical expression for the time constant is formulated and can be expressed by (2) where K is a constant varying from 0.7 to 1.2 depending on the initial charge of the capacitance. r_{ON} represents the NMOS transistor average ON resistance.

The proposed one shot timer is simulated with values for R_{ext} and C_{ext} set to 30 kΩ and 1 nF respectively. The time constant is expected to be between 26 μs and 37 μs by calculation. The above calculation is confirmed from
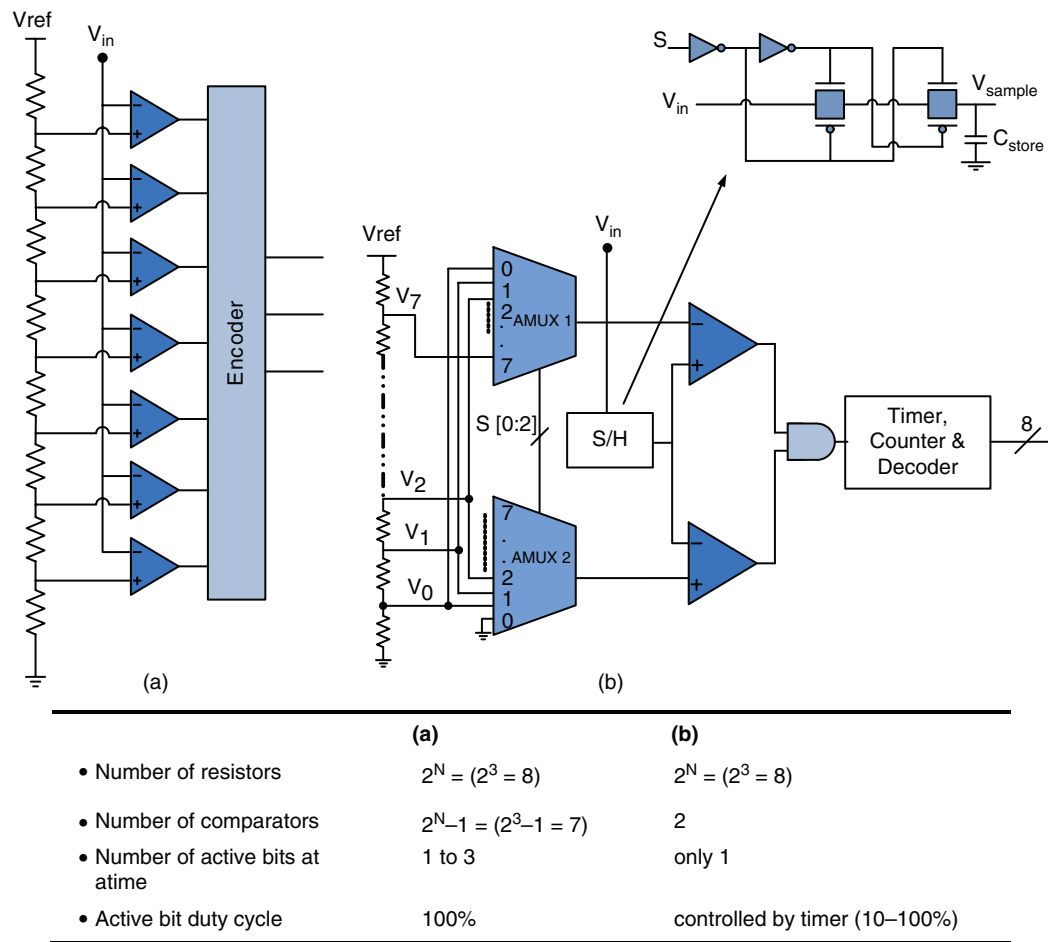
	(a)	(b)
• Number of resistors	$2^N = (2^3 = 8)$	$2^N = (2^3 = 8)$
• Number of comparators	$2^N - 1 = (2^3 - 1 = 7)$	2
• Number of active bits at atime	1 to 3	only 1
• Active bit duty cycle	100%	controlled by timer (10–100%)

Fig. 4. Comparison of (a) 3-bit flash ADC and (b) proposed interface circuit.

Fig. 5. Proposed interface circuit design.

(a) The AMUX's switch through the reference voltage until both comparators give "1" output. Color is not identified yet.

(b) The color value is successfully identified which is indicated by "1" output at the AND gate.
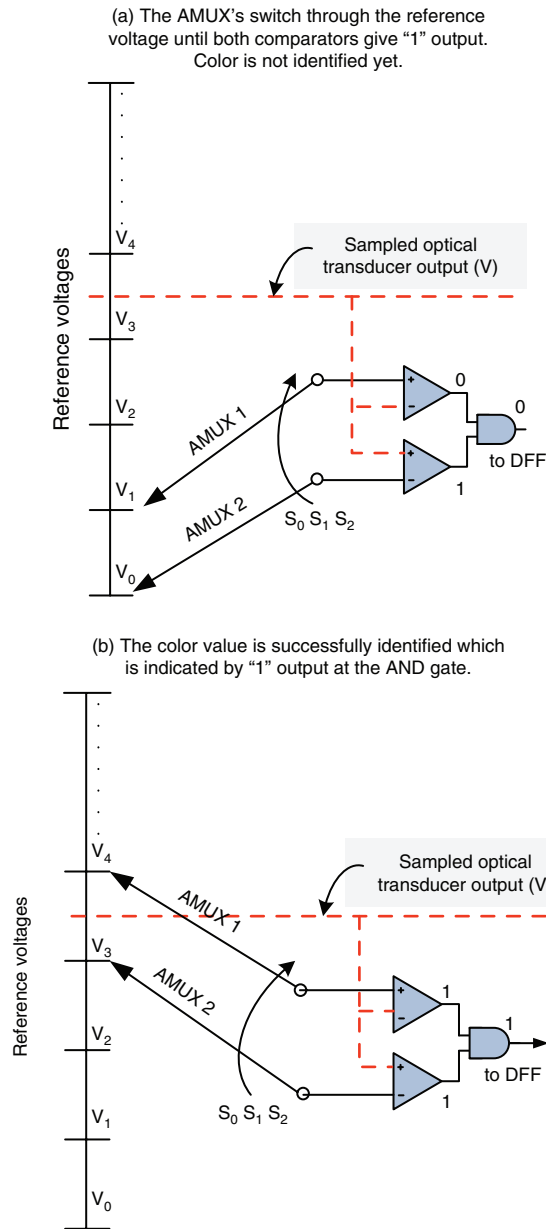
Fig. 6. Conceptual diagram illustrating operation of the proposed interface circuit.
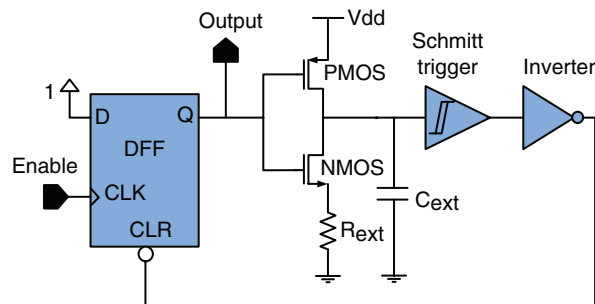

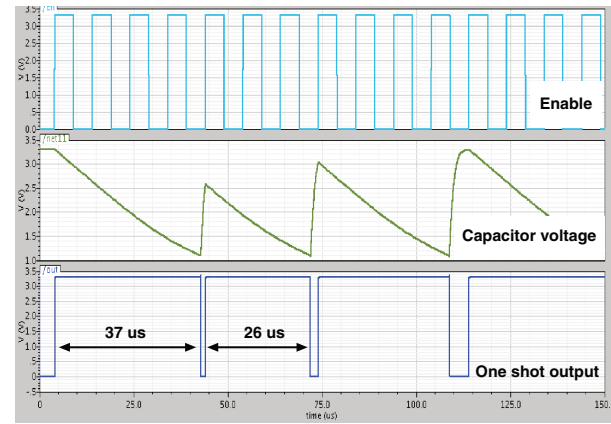**Fig. 7.** Proposed timer design.

Fig. 8. Simulation result of the proposed one-shot design.

the simulation result as shown in Figure 8. This block is optional because it merely controls the duration of the active bits and doesn't affect the basic functionality of the design.
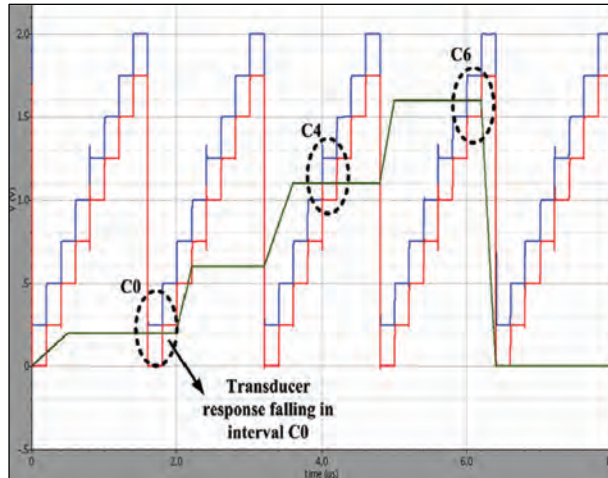
4. SIMULATION RESULT

The proposed interface circuit from Figure 5 is validated by simulation using Cadence Design System software and the result is shown in Figure 9. The multi-bit digital output represents color of the detected light and which is obtained by comparing the light transducer voltage against pre-stored reference levels. For simulation purpose the optical transducer signal is replaced by a voltage source and the reference intervals representing the 8 different colors are set as shown in Table I.

Figure 9(a) illustrates the staircase like signals produced by the AMUXs and the transducer signal (i.e., green). In any detection cycle, the AMUXs keep on switching through the reference ladders until the input voltage from the transducer falls in the interval of the pre-stored reference voltages (i.e., for yellow color detection, the transducer voltage has to fall in the interval 1.25–1.5 V). When the right interval is found, the color represented by the interval is said to be detected. The digital outputs are designated as C0, C1, C2, up to C7 representing 8 different colors. For instance, the circled regions in Figure 9(a) represent the transducer voltage falling inside the interval

Table I. Reference level interval created for color comparison.

	C0	C1	C2	C3	C4	C5	C6	C7	Voltage intervals (V)
Violet	1	0	0	0	0	0	0	0	0.0–0.25
Blue	0	1	0	0	0	0	0	0	0.25–0.5
Cyan	0	0	1	0	0	0	0	0	0.5–0.75
Green	0	0	0	1	0	0	0	0	0.75–1.0
Yellow-green	0	0	0	0	1	0	0	0	1.0–1.25
Yellow	0	0	0	0	0	1	0	0	1.25–1.5
Orange	0	0	0	0	0	0	1	0	1.5–1.75
Red	0	0	0	0	0	0	0	1	1.75–2.0

(a) Signal at AMUX 1, AMUX 2 and Light transducer from Cadence simulation.

(b) Final digital output representing 8 colors. Circled regions represent detection of Violet, Yellow-green and Orange colors.
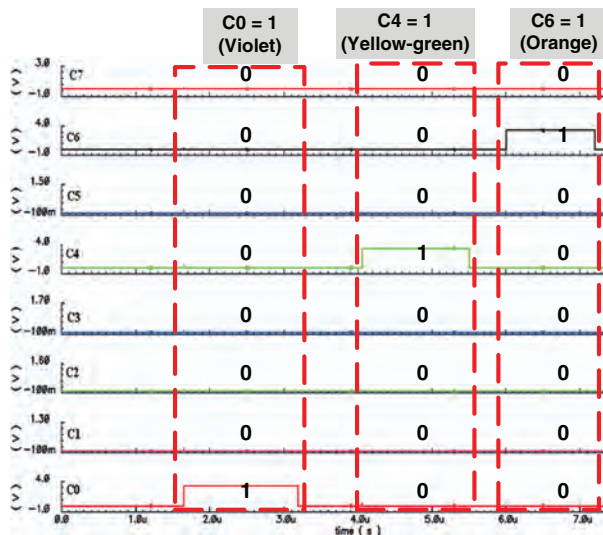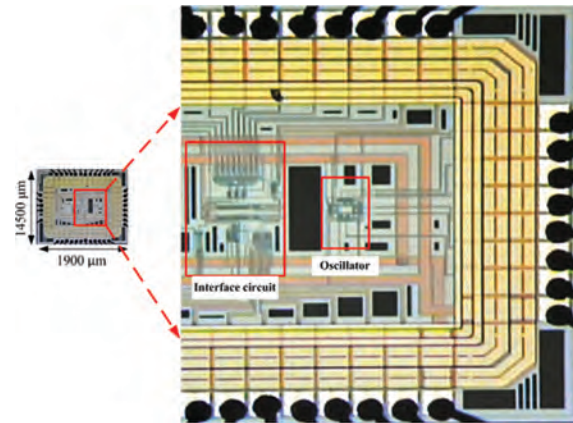

Fig. 9. Cadence simulation result of proposed interface circuit.

created by the two AMUXs. Figure 9(b) shows the corresponding color representing bit having a high ("1") digital output while the rest have a low ("0") output. As such, when the input voltage from the transducer falls into the first interval, C0 (Violet) indicator goes high while the rest of the bits (C1 to C7) remain low as shown on Figure 9(b). Similar cases are also depicted in the figure with Yellow-green and Orange colors (C4, and C6 respectively) being detected at different times.

The transducer value is changed continuously to simulate real life color changes e.g., continuous color changes in a pH solution or fluorescence emission phenomenon. The simulation result demonstrates that the optical detector circuit is fully autonomous, i.e., it can track the color change without any need of interference from a user.

(a) Micrograph of the fabricated chip. Fabricated prototype consists of photodiode and preamplifier unit (for later characterization); an interface circuit block and an oscillator block (internal clock generator circuit)

(b) Micrograph of the fabricated chip.

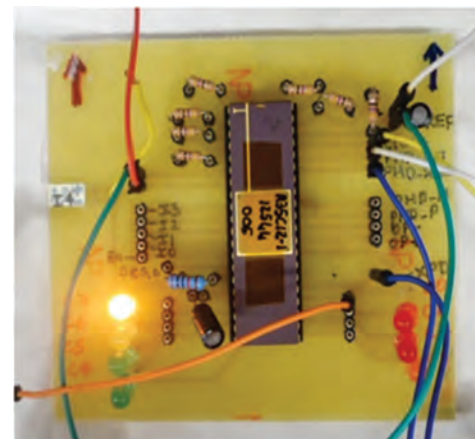(c) Fabricated chip with external resistor ladder for experimental testing.

Fig. 10. Fabricated prototype and its experimental setup.

5. EXPERIMENTAL RESULTS FROM FABRICATED PROTOTYPE

The proposed interface circuit is fabricated in a CMOS standard process using the 0.35 μm Austria Microsystems technology. Micrograph of the fabricated chip and its

(a) Digital output for an optical transducer value V = 480 mV.
Bit C1 blinks indicating bluecolor detected.

(b) Digital output for an optical transducer value V = 1.21 V.
C4 blinks indicating Yellow-Green color detected.

(c) Digital output for an optical transducer value V = 0.1.9 V.
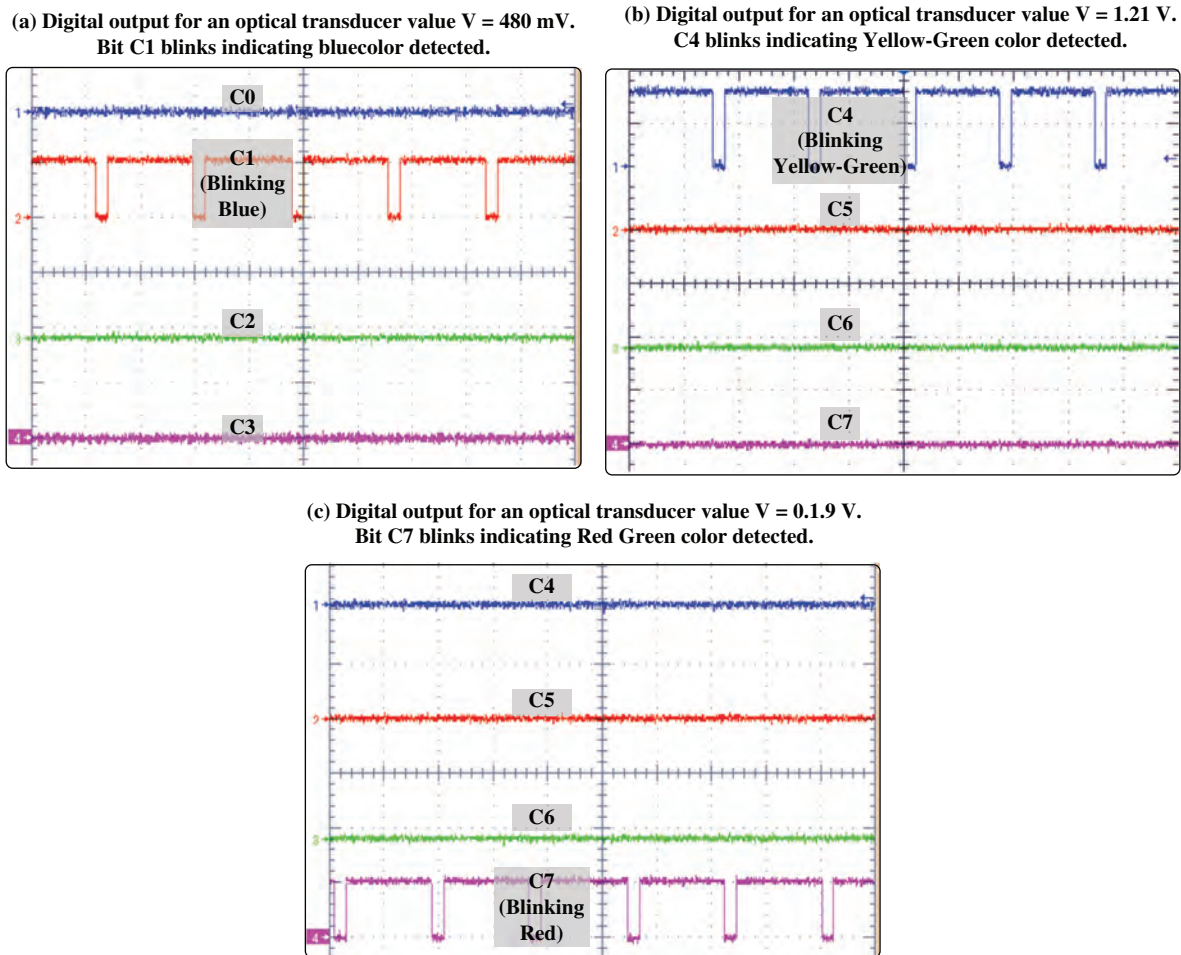Bit C7 blinks indicating Red Green color detected.

Fig. 11. Experimental result from fabricated prototype. (Only four bits of the digital output are shown at a time from a 4 channel oscilloscope). Active bit duty cycle is set to be ≈80%.

Table II. Comparison table.

Ref.	Power consumption	CMOS technology	Final output signal	Remark
[8]	800 μW	AMI 1.5 μm	Analog voltage output	Further processing is needed to identify color (e.g., Red, Blue... etc.) - Microcontroller (ADC + DSP, memory units are needed)
[19]	–	DIMES 1.6 μm	Digital output	Microcontroller (DSP, memory units are needed) to identify color
[20]	400 μW	n-well 0.7 μm	Digital output	Microcontroller (DSP, memory units are needed) to identify color
[21]	1250 μW	DIMES 1.6 μm	Frequency output	PC or microcontroller (DSP, memory units are needed are needed) to identify color
This work	37 μW	AMS 0.35 μm	Detected color (Digital word)	Color is identified readily - No further processing is needed

testing setup is shown in Figure 10. The fabricated prototype, as shown in Figure 10(a), consists of photodiode and preamplifier unit (for later characterization purpose); an interface circuit block (the focus of this paper) and an oscillator block (internal clock generator circuit). The design is done in such a way that a separate characterization of all the blocks is possible. Figure 10(c) depicts the PCB testing platform for the interface circuit block of the fabricated chip.

Experimental testing of the fabricated prototype is conducted using Instek GW voltage source, Tektronics TDS 5104 Digital phosphor oscilloscope (4 channel display) and Agilent waveform generator. Figures 11(a) to (c) shows the detected color output (digital output) from the chip for different optical transducer response as captured from the TDS oscilloscope screen. Since the oscilloscope has only 4 channels, 4 out of the 8 bits (indicator LEDs) are shown at a time. Figure 11(a) shows a high C1 output ("1"), indicating the detected color falls in the interval 250 mV to 500 mV (which, referring to Table I, is a Blue color). Similarly, Figures 11(b) and (c) show the digital output for an optical transducer voltage of 1.6 V and 1.9 V respectively. The output bits refresh (the indicator LEDs blink) every detecting cycle preparing for a new sampled input from the optical transducer.

6. PROPOSED DESIGN SPECIFICATION AND COMPARISON

The interface circuit is a mixed signal design including both analog and digital blocks. The whole chip has an area of 1900 μm by 1500 μm, operating voltage of 3.3 V and power consumption of 37 μW which is mainly consumed by the analog components of the interface circuit. Furthermore, the fabricated prototype includes a photodiode and preamplifier unit for later characterization purpose and an oscillator block (internal clock generator circuit) to serve the purpose of clock generation for the interface circuit. The comparison Table II summarizes the performance of few previously proposed optical sensor systems for similar applications.

7. CONCLUSION

In this paper a CMOS based interface circuit for a smart optical sensor is presented. Simulation and experimental data from fabricated chip using 0.35 um CMOS process are discussed and validated the proposed concept. From the results, it was shown that the architecture is able to capable to efficiently identify 8 different colors while featuring ultra-low power consumption (37 μW). The proof of concept design presented here is mainly based on components directly available from the foundry library. Better performance can be further obtained by using customized blocks. The main advantage of the proposed architecture is mainly attributed to the minimization of the number

of components. Moreover, it produces immediate or real time response unlike many optical sensor systems for similar applications which uses external processors like spectrometer, microcontrollers, computer or image processing devices to produce a final color output. The presented interface circuitry along with a light transducer and a clock generator is an ideal candidate as a self-contained, portable pH measuring device for biomedical and environmental applications.

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