Research Article

An SIMD Programmable Vision Chip with High-Speed Focal Plane Image Processing

Dominique Ginhac, Jérôme Dubois, Michel Paindavoine, and Barthélemy Heyrman

Laboratoire d'Electronique Informatique et Image (LE2I), UMR CNRS 5158, Health-STIC Federative Research Institute (IFR100), Burgundy University, 21078 Dijon, France

Correspondence should be addressed to Dominique Ginhac, dginhac@u-bourgogne.fr

Received 1 March 2008; Revised 13 June 2008; Accepted 12 November 2008

Recommended by Dragomir Milojevic

A high-speed analog VLSI image acquisition and low-level image processing system are presented. The architecture of the chip is based on a dynamically reconfigurable SIMD processor array. The chip features a massively parallel architecture enabling the computation of programmable mask-based image processing in each pixel. Extraction of spatial gradients and convolutions such as Sobel operators are implemented on the circuit. Each pixel includes a photodiode, an amplifier, two storage capacitors, and an analog arithmetic unit based on a four-quadrant multiplier architecture. A 64 × 64 pixel proof-of-concept chip was fabricated in a 0.35 μm standard CMOS process, with a pixel size of 35 μm × 35 μm. A dedicated embedded platform including FPGA and ADCs has also been designed to evaluate the vision chip. The chip can capture raw images up to 10 000 frames per second and runs low-level image processing at a framerate of 2 000 to 5 000 frames per second.

Copyright © 2008 Dominique Ginhac et al. This is an open access article distributed under the Creative Commons Attribution License, which permits unrestricted use, distribution, and reproduction in any medium, provided the original work is properly cited.

1. INTRODUCTION

Today, digital cameras are rapidly becoming ubiquitous, due to reduced costs and increasing demands of multimedia applications. Improvements in the growing digital imaging world continue to be made with two main image sensor technologies: charge-coupled devices (CCDs) and CMOS sensors. Historically, CCDs have been the dominant image-sensor technology. However, the continuous advances in CMOS technology for processors and DRAMs have made CMOS sensor arrays a viable alternative to the popular CCD sensors. This led to the adoption of CMOS image sensors in several high-volume products, such as webcams, mobile phones, PDAs, for example. Furthermore, new recent technologies provide the ability to integrate complete CMOS imaging systems at focal plane, with analog-to-digital conversion, memory and processing [1–5]. By exploiting these advantages, innovative CMOS sensors have been developed and have demonstrated fabrication cost reduction, low power consumption, and size reduction of the camera [6–8].

The main advantage of CMOS image sensors is the flexibility to integrate processing down to the pixel level. As CMOS image sensors technologies scale to 0.18 μm processes and under, processing units can be realized at chip level (system-on-chip approach), at column level by dedicating processing elements to one or more columns, or at pixel-level by integrating a specific unit in each pixel or local of neighboring pixels. Most of the researches deal with chip and column level [9–12]. Indeed, pixel-level processing is generally dismissed because pixel sizes are often too large to be of practical use. However, as CMOS scales, integrating a processing element at each pixel or group of neighboring pixels becomes more feasible since the area occupied by the pixel transistors decreases, leading to an acceptable small pixel size. A fundamental tradeoff must be made between three dependent and correlated variables: pixel size, processing element area, and fill-factor. This implies various points of view:

1. for a fixed fill-factor and a given processing element area, the pixel size is reduced with technology improvements, as a consequence, reducing pixel size increases spatial resolution for a fixed sensor die size;
2. for a fixed pixel size and a given processing element area, the photodiode area and the fill-factor increase as technology scales since the area occupied by the
pixel transistors in each processing element decreases. It results in better sensibility, higher dynamic range and signal-to-noise ratio;

(3) for a fixed pixel size and a given fill-factor, the processing element can integrate more functionalities since the transistors require less area as technology scales. Consequently, the image processing capabilities of the sensor increase.

In summary, each new technology process offers (1) to integrate more processing functions in a given silicon area, or (2) to integrate the same functionalities in a smaller silicon area. This can benefit the quality of imaging in terms of resolution, noise, for example, by integrating specific processing functions such as correlated double sampling [13], antiblooming [14], high dynamic range [15], and even all basic camera functions (color processing functions, color correction, white balance adjustment, gamma correction) onto the same camera-on-chip [16]. Furthermore, employing a processing element per pixel offers the ability to exploit the high speed imaging capabilities of the CMOS technology by achieving massively parallel computations [17–20].

In this paper, we discuss hardware implementation issues of a high-speed CMOS imaging system embedding low-level image processing. For this purpose, we designed, fabricated, and tested a proof-of-concept $64 \times 64$ pixel CMOS analog sensor with per-pixel programmable processing element in a standard $0.35 \mu m$ double-poly quadruple-metal CMOS technology. The rest of the paper is organized as follows. Section 2 is dedicated to the description of the high speed algorithms embedded at pixel-level. Section 3 is a general description of the characteristics of the sensor. These characteristics are well detailed in Section 4, which talks about the design of the circuit, with a full description of the main components such as the photodiode structure, the embedded analog memories, and the arithmetic unit are successively described. In Section 5, we describe the test hardware platform and the chip characterization results, including an analysis of the fixed pattern noise. Finally, some experimental results of high-speed image acquisition with pixel-level processing are provided in Section 6 of this paper.

2. HIGH SPEED FOCAL PLANE IMAGE-PROCESSING CAPABILITIES

In an increasingly digital world, the most part of imaging systems have become almost entirely digital, using only an analog-to-digital (ADC) between the sensor and the processing operators. However, low-level image processing usually involves basic operations using local masks. These local operations are spatially dependent on other pixels around the processed pixel, since the same type of operations is applied to a very large dataset, these low-level tasks are computationally intensive and require a high bandwidth between the image memory and the digital processor. In this case, an analog or a mixed-approach can offer superior performance leading to a smaller, faster, and lower power solution than a digital processor [21]. Low-level image processing tasks are inherently pixel-parallel in nature. Integrating a processing element within each pixel based on a single instruction multiple data (SIMD) architecture is a natural candidate to cope with the processing constraints [18]. This approach is quite interesting for several aspects. First, SIMD image-processing capabilities at focal plane have not been fully exploited because the silicon area available for the processing elements is very limited. Nevertheless, this enables massively parallel computations allowing high framerates up to thousands of images per second. The parallel evaluation of the pixels by the SIMD operators leads to processing times, independent of the resolution of the sensor. In a classical system, in which low-level image processing is externally implemented after digitization, processing times are proportional to the resolution leading to lower framerates as resolution increases. Several papers have demonstrated the potentially outstanding performance of CMOS image sensors [22–24]. Krymski et al. [22] describe a high speed (500 frames/s) large format $1024 \times 1024$ active pixel sensor (APS) with $1024$ ADCs. Stevanovic et al. [23] describe a $256 \times 256$ APS which achieves more than 1000 frames/s with variable integration times. Kleinfelder et al. [24] describe a $352 \times 288$ digital pixel sensor (DPS) with per pixel bit parallel ADC achieving 10 000 frames/s or 1 Giga-pixels/s.

Secondly, the high speed imaging capability of CMOS image sensors can benefit the implementation of new complex applications at standard rates and improve the performance of existing video applications such as motion vector estimation [25–27], multiple capture with dynamic range [28–30], motion capture [31], and pattern recognition [32]. Indeed, standard digital systems are unable to operate at high framerates, because of the high output data rate requirements for the sensor, the memory, and the processing elements. Integrating the memory and processing with the sensor on the same chip removes the classical input output bottleneck between the sensor and the external processors in charge of processing the pixel values. Indeed, the bandwidth of the communication between the sensor and the external processors is known as a crucial aspect, especially with high resolution sensors. In such cases, the sensor output data flow can be very high, and needs a lot of hardware resources to convert, process and transmit a lot of information. So, integrating image processing at the sensor level can alleviate the high data rate problem because the pixel values are pre-processed on-chip by the SIMD operators before sending them to the external world via the communication channel. This will result in data reduction, which allows sending the data at lower data-rates, and reduces the effect of the computational-load bottleneck.

Thirdly, one of the main drawbacks to design specific circuits integrating sensing and processing on the same chip is that these vision chips are often built as special-purpose devices, performing specific and dedicated tasks, and not reusable in another context [33]. So, it can be widely beneficial to integrate a versatile device, whose functionality can be easily modified. Moreover, except the basic operations such as convolutions with small masks, the majority of computer vision algorithms require the sequential execution of different successive low-level image processing on the
same data. So, each processing element must be built around a programmable execution unit, communication channels, and local memories dedicated to intermediate results. Because of the very limited silicon area, the processing units are necessarily very simple, providing the best compromise between various factors such as versatility, complexity, parallelism, processing speeds and resolution.

To sum up, the flexibility to integrate processing down to the pixel level allows us to rearchitect the entire imaging system to achieve much higher performances [34]. The key idea is (1) to capture images at a very high framerate, (2) to process the data on each pixel with a SIMD programmable architecture exploiting the high on-chip bandwidth between the sensor, the memory and the elementary processors, and (3) to provide results at the best framerate depending on the complexity of the image processing. In this paper, we present our approach to the design of a massively parallel, SIMD vision chip based implementing low level image processing based on local masks. Our analog processing operators are fully programmable devices by dynamic reconfiguration, and can be viewed as a software-programmable image processor dedicated to low-level image processing. The main objectives of our design are (1) to evaluate the potential for high-speed snapshot imaging and, in particular, to reach a 10 000 frames/s rate, (2) to demonstrate a versatile and reconfigurable processing unit at pixel level, and (3) to provide an original platform for experimenting with low-level image processing algorithms that exploit high-speed imaging.

3. DESCRIPTION OF THE ARCHITECTURE

The proof-of-concept chip presented in this paper is depicted in Figure 1. The core includes a two-dimensional array of 64 × 64 identical processing element (PE). It follows the single instruction multiple data (SIMD) computing paradigm. Each of the PE is able to convolve the pixel value issued from the photodiode by applying a set of mask coefficients to the image pixel values located in a small neighborhood. The key idea is that a global control unit can dynamically reconfigure the convolution kernel masks and then implements the most part of low-level image processing algorithms. This confers the functionality of programmable processing devices to the PEs embedded in the circuit. Each individual PE includes the following elements.

(i) A photodiode dedicated to the optical acquisition of the visual information and the light-to-voltage transduction.

(ii) Two analog memory, amplifier and multiplexer structures called [AM]², which serve as intelligent pixel memories and are able to dissociate the acquisition of the current frame in the first memory and the processing of the previous frames in the second memory.

(iii) An analog arithmetic unit named A²U based on four analog multipliers, which performs the linear combination of the four adjacent pixels using a 2 × 2 convolution kernel.

In brief, each PE includes 38 transistors integrating all the analog circuitry dedicated to the image processing algorithms. The global size of the PE is 35 μm × 35 μm (1225 μm²). The active area of the photodiode is 300 μm², giving a fill-factor of 25%. The chip has been realized in a standard 0.35 μm double-poly quadruple-metal CMOS technology and contains about 160 000 transistors on a 3.67 mm × 3.77 mm die (13.83 mm²). The chip also contains test structures on the bottom left of the chip. These structures are used for detailed characterization of the photodiodes and processing units.
Based on this design concept, this forces a rethinking of the spatial distribution of the processing resources, so that each computational unit can easily use a programmable neighborhood of pixels. For this purpose, the pixels are mirrored about the horizontal and the vertical axes in order to share the different analog arithmetic units (A2Us). As example, a block of $2 \times 2$ pixels is depicted in Figure 1. The main feature of its innovative distribution is to optimize the compactness of the metal interconnections with pixels, to contribute to a better fill factor, and to provide generality of high-speed processing based on neighborhood of pixels.

### 4.2. Analog memory, amplifier and multiplexer: $[AM]^2$

In order to increase the algorithmic possibilities of the architecture, the key point is the separation of the acquisition of the light inside the photodiode and the readout of the stored value at pixel-level [41]. Thus, the storage element should keep the output voltage of the previous frames whereas the sensor integrates photocurrent for a new frame. So, we have designed and implemented dedicated pixels including a light sensitive structure and two specific circuits called analog memory, amplifier, and multiplexer ($[AM]^2$), as shown in Figure 2.

The system has five successive operation modes: reset, integration, storage, amplification, and readout. All these phases are externally controlled by global signals common to the full array of pixels. They all occur in parallel over the sensor (snapshot mode) in order to avoid any distortion due to a row-by-row reset. In each pixel, the photosensor is an $N$-type photodiode associated with a PMOS transistor reset. This switch resets the integrating node to the fixed voltage $V_{dd}$. The pixel array is held in the reset mode until the $init$ signal raises, turning the PMOS transistor off. Then, the photodiode discharges for a fixed period, according to the incidental luminous flow. The first NMOS transistor acts as a transconductance, producing the voltage $V_{ph}$, directly proportional to the incident light intensity. The integrated voltage is polarized around $V_{dd}/2$ by the second NMOS transistor. The calibration of the structure is ensured by the positive reference bias voltage ($V_{bias} = 1.35 \text{V}$).

Following the acquisition stage, two identical subcircuits $[AM]^2$ (with $i = 1, 2$) take place to realize the storage phase of $V_{ph}$. Each $[AM]^2$ includes three pairs of NMOS and PMOS transistors and a capacitor which acts as an analog memory. The subcircuit $[AM]^2$ is selected when the $st_i$ signal is turned on. Then, the associated analog switch is open allowing the integration of the photogenerated current in the corresponding $C_i$ capacitor. Consequently, the capacitors are able to store the pixel value during the frame capture from one of the two switches. The capacitors are implemented with double-polysilicon. The size of the capacitors is as large as possible in order to respect the fill-factor and the pixel-size requirements. The capacitors values are about 40 fF. They are able to store the pixel signal for 20 milliseconds with an error lower than 4%. Behind the storage subcircuit, a basic CMOS inverter is integrated. This inverter serves as a linear high-gain amplifier since the pixel signal is polarized.
the stored values in the capacitors \( C_i \).

\[ V_{dd}/2 \]

\[ V_{ph} \]

\[ V_{out1} \]

\[ V_{out2} \]

**Figure 3:** High-speed sequence capture with basic image processing.

around \( V_{dd}/2 \). Finally, the last phase consists in the readout of the stored values in the capacitors \( C_i \). The integrated voltage across the capacitor \( C_i \) can be readout on the output \( out_i \) through one of the two switches, controlled by the \( r_i \) signals.

Figure 3 describes the experimental results of successive acquisitions in an individual pixel. The acquisitions occur when one of the two signals \( s_1 \) or \( s_2 \) goes high. The two combinations of acquisitions are presented in this example. After the first reset, \( s_2 \) is followed by \( s_1 \) whereas the inverted sequence of acquisitions is realized after the second reset. The signal \( V_{ph} \) gives the voltage corresponding to the incidental illumination on the pixel and the two outputs (\( out_1 \) and \( out_2 \) give the voltage stored in each of the capacitors when the associated readout signal raises.

One of the main advantages of the two \([AM]^2\) structures is that the capture sequence can be made in the first memory in parallel with a readout sequence and/or processing sequence of the previous image stored in the second memory, as shown in Figure 4.

Such a strategy has several advantages.

1. The framerate can be increased (up to \( 2 \times \)) without reducing the exposure time.
2. The image acquisition is time-decorrelated from image processing, implying that the architecture performance is always the highest, and the processing framerate is maximum.
3. A new image is always available without spending any integration time.

**4.3. Analog arithmetic unit: A^2U**

When designing a pixel-level processing unit, you should consider adopting efficient strategies to minimize the silicon area occupied by the processor. To that end, we designed an analog arithmetic unit (A^2U) which is able to perform convolution of the pixels with a \( 2 \times 2 \) dynamic kernel. This unit is based on four-quadrant analog multipliers [42, 43] named M1, M2, M3, and M4, as illustrated in Figure 5. Each multiplier requires 5 transistors. So, the transistor count of the complete unit is only 22 transistors. The last two transistors not depicted on the Figure 5 serve as an output switch, driven by the column signal. It features relative small area, simplicity, and high speed. These characteristics make it an interesting choice in low-level image processing embedded at focal plane. Each multiplier \( M_i \) (with \( i = 1, \ldots, 4 \)) takes two analog signals \( V_{i1} \) and \( V_{i2} \) and produces an output \( V_{iS} \) which is their product. The outputs of multipliers are all interconnected with a diode-connected transistor employed as load. Consequently, the global operation result at the \( V_S \) point is a linear combination of the four products \( V_{iS} \). Image processing operations such as spatial convolution can be easily performed by connecting the inputs \( V_{i1} \) to the kernel coefficients and the inputs \( V_{i2} \) to the corresponding pixel values.

In order to keep the analysis simple, it is assumed in this section that the contribution of parasitic capacitances is negligible. Considering the MOS transistors operating in subthreshold region, the output node \( V_{iS} \) of a multiplier can be expressed as a function of the two inputs \( V_{i1} \) and \( V_{i2} \) as follows:

\[
M = \frac{k_r - 1}{2V_{THN} + V_{THP}} \approx 8.07/V. 
\]

The important value of the coefficient \( M \) gives to the structure a good robustness by limiting the impact of the second-order intermodulation products. The first consequence is
a better linearity of our multiplier design integrating only 5 transistors.

The theoretical analysis has been validated by an experimental study realized on the test structures embedded on the chip. Figure 6 shows the experimental measures obtained with two cosine signals as inputs of the multiplier structure.

\[ V_{i1} = A \cos(2\pi f_1) \quad \text{with} \quad f_1 = 2.5 \text{kHz}, \]
\[ V_{i2} = B \cos(2\pi f_2) \quad \text{with} \quad f_2 = 20 \text{kHz}. \] (3)

In an ideal case, the voltage \( V_S \) at the output of the multiplier can be expressed as

\[ V_S = \frac{AB}{2} \left[ \cos(2\pi(f_2 - f_1)) + \cos(2\pi(f_2 + f_1)) \right]. \] (4)

The frequency spectrum, represented in Figure 6(b) contains two main frequencies (17.5 kHz and 22.5 kHz) around the carrier frequency. The residues which appear in the spectrum are known as intermodulation products. Intermodulation is caused by nonlinear behavior of the structure (around 10 kHz and 30 kHz) and the insulation defects of input pads (at 40 kHz). Nevertheless, the amplitude of these intermodulation products is significantly lower than the two main frequencies. Indeed, at 40 kHz, the level of intermodulation is 9 dB under the level of the main frequencies. Therefore, the contribution of the insulation defect is eight times smaller than the main signals. Furthermore, the experimental measures highlighted that the linearity of the multiplier is maximum for input signals with amplitude range between 0.6 V and 2.6 V. This corresponds to the typical range of values coming from the pixel since the \([AM]^2\) structures provide values around \( V_{dd}/2 = 1.65 \text{V} \).

5. CHIP CHARACTERIZATION

An experimental 64 \( \times \) 64 pixel image sensor has been developed in a 0.35\( \mu \text{m} \), 3.3 V, standard CMOS process with poly-poly capacitors. Its functional testing and its characterization were performed using a specific hardware platform. The hardware part of the imaging system contains a one million Gates Spartan-3 FPGA board with 32MB SDRAM embedded. This FPGA board is the XSA-3S1000 from XESS Corporation. An interface acquisition circuit includes three ADCs from analog device (AD9048), high-speed LM6171 amplifiers and others elements such as the motor lens. Figure 7 shows the schematic and some pictures of the experimental platform.

5.1. Electrical characterization

The sensor was quantitatively tested for conversion gain, sensitivity, fixed pattern noise, thermal reset noise, output levels disparities, voltage gain of the amplifier stage, linear flux, and dynamic range. Table 1 summarizes the main chip properties and the characterization results.

To determine these values, the sensor included specific test pixels in which some internal node voltages can be directly read. The test equipment hardware is based on a light generator with wavelength of 400 nm to 1100 nm. The sensor conversion gain was evaluated to 54 \( \mu \text{V/e}^{-}\) RMS with a sensitivity of 0.15 V/\text{lux.s}, thanks to the octagonal shape of the photodiode and the fill-factor of 25%. At 10 000 frames/s, measured nonlinearity is 0.12% over a 2 V range. These performances are similar to the sensor described in [24]. According to the experimental results, the voltage gain of the amplifier stage of the two \([AM]^2\) is \( A_V = 12 \) and the disparities on the output levels are about 4.3%.

5.2. Fixed pattern noise

Image sensors always suffer from technology related nonidealities that can limit the performances of the vision system. Among them, fixed pattern noise (FPN) is the variation in output pixel values, under uniform illumination, due to
device and interconnect mismatches across the image sensor. Two main types of FPN occur in CMOS sensors. First, offset FPN which takes place into the pixel is due to fluctuations in the threshold voltage of the transistors. Second, the most important source of FPN is introduced by the column amplifiers used in standard APS systems. In our approach, the layout is symmetrically built in order to reduce the offset FPN among each block of four pixels and to ensure uniform spatial sampling, as already depicted in the layout of a 2 × 2 pixel block in Figure 1.

Furthermore, our chip does not include any column amplifier since the amplification of the pixel values takes place into the pixel by means of an inverter. So, the gain FPN is very limited and only depends on the mismatch of the two transistors. FPN can be reduced by correlated double sampling (CDS). To implement CDS, each pixel output needs to be read twice, once after reset and a second time at the end of integration. The correct pixel signal is obtained by subtracting the two values. A CDS can be easily implemented in our chip. For this purpose, the first analog memory stores the pixel value just after the reset signal and the second memory stores the value at the end of integration. Then, at the end of the image acquisition, the two values can be transferred to the FPGA, responsible for producing the difference. In Figure 8 the two images show fixed pattern noise with and without CDS using a 1 millisecond integration time. On the left image, the FPN is mainly due to the random variations in the offset voltages of the pixel-level analog structures. The
8 EURASIP Journal on Embedded Systems

Figure 8: Images of fixed pattern noise (a) without CDS and (b) with CDS for an integration time of 1 millisecond.

Experimental benchmarks of our chip reveal an FPN value of 225 μV RMS. The right picture shows the same image after analog CDS, performed as described above. The final FPN has been reduced by a factor of 34 to 6.6 μV. In the rest of the results, CDS has not been implemented since FPN has low values. Only, an entire dark image is substracted from the output images on the FPGA. Focus has been made on the development of low-level image processing using the two analog memories and the associated processing unit.

6. HIGH-SPEED IMAGE PROCESSING APPLICATIONS

In this section, we provide experimental results of image processing implemented on our high-speed vision chip. First, we demonstrate the possibility of acquisition of raw images at different framerates, up to 10 000 frames/s. Secondly, we present an implementation of edge detection, based on the well-known Sobel operator.

6.1. Sample images

The prototype chip was used for acquisition of raw images. First, sample raw images of stationary scenes were captured at different framerates, as shown in Figure 9. In the three views, no image processing is performed on the video stream, except for amplification of the photodiodes signal. From left to right, we can see a human face obtained at 1 000 frames/s, a static electric fan at 5 000 frames/s, and an electronic chip at 10 000 frames/s.

Figure 10 represents different frames of a moving object, namely, a milk drop splashing sequence. In order to capture the details of such a rapidly moving scene, the sensor operates at 2 500 frames/s and stores a sequence of 50 images. The frames 1, 5, 10, 15, 20, 25, 30, and 40 are shown in the figure.

6.2. Sobel operator

The characteristics of our sensor, especially the analog processing unit, make it extremely useful for low-level image processing based on convolution masks. In this paragraph, we report an edge detector, the Sobel detector. The Sobel operator estimates the gradient of a 2D image. This algorithm is used for edge detection in the preprocessing stage of computer vision systems. The classical algorithm uses a pair of 3 × 3 convolution kernels (5), one to detect changes along the vertical axis \( h_1 \) and another one to detect horizontal contrast \( h_2 \). For this purpose, the algorithm performs a convolution between the image and the sliding convolution mask over the image. It manipulates 9 pixels for each value to produce. The value corresponds to an approximation of the gradient centered on the processed image area:

\[
h_1 = \begin{pmatrix} -1 & 0 & 1 \\ -2 & 0 & 2 \\ -1 & 0 & 1 \end{pmatrix}, \quad h_2 = \begin{pmatrix} -1 & -2 & -1 \\ 0 & 0 & 0 \\ 1 & 2 & 1 \end{pmatrix}. \tag{5}\]

The structure of our architecture is well adapted to the evaluation of the Sobel algorithm. It leads to the result directly centered on the photosensor and directed along the natural axes of the image. The gradient is computed in each pixel of the image by performing successive linear combinations of the 4 adjacent pixels. For this purpose, each 3 × 3 kernel mask is decomposed into two 2 × 2 masks that successively operate on the whole image. For the kernel \( h_1 \), the corresponding 2 × 2 masks are:

\[
m_1 = \begin{pmatrix} -1 & 0 \\ -1 & 0 \end{pmatrix}, \quad m_2 = \begin{pmatrix} 0 & 1 \\ 0 & 1 \end{pmatrix}. \tag{6}\]

Figure 11 represents the 3 × 3 mask centered on the pixel \( \text{ph}_5 \). Each octagonal photodiode \( \text{ph}_i (i = 1, \ldots, 9) \) is associated with a processing element \( \text{PE}_i \), represented with a circle on the figure. Each \( \text{PE}_i \) is positioned on the bottom right of its photodiode, as in the real layout of the circuit (see Figure 1). The first mask \( m_1 \) contributes to evaluate the following series of operations for the four \( \text{PE}_{i5}: \)

\[
V_{11} = -(V_{\text{ph}_1} + V_{\text{ph}_4}), \quad V_{12} = -(V_{\text{ph}_2} + V_{\text{ph}_5}), \quad V_{14} = -(V_{\text{ph}_4} + V_{\text{ph}_7}), \quad V_{15} = -(V_{\text{ph}_5} + V_{\text{ph}_8}). \tag{7}\]
Figure 9: Various raw images acquisition at 1000, 5000 and 10000 frames/s.

Figure 10: A 2500 frames/s video sequence of a milk drop splashing.
and the second mask $m_2$ computes:

$$
\begin{align*}
V_{21} & = + (V_{ph_5} + V_{ph_7}), \\
V_{22} & = + (V_{ph_5} + V_{ph_6}), \\
V_{24} & = + (V_{ph_3} + V_{ph_6}), \\
V_{25} & = + (V_{ph_2} + V_{ph_9})
\end{align*}
$$

with $V_{ij}$ corresponding to the result provided by the processing element $PE_j$ ($j = 1, 2, \ldots, 9$) with the mask $m_i$ ($i = 1, 2$), and $V_{ph_k}$ ($k = 1, 2, \ldots, 9$), the voltages representing the incidental illumination on each photodiode $ph_k$. Then, the evaluation of the gradient at the center of the mask can be computed by summing the different values on the external FPGA. Note that $V_{12} = -V_{21}$ and $V_{15} = -V_{24}$. So, the final sum can be simplified and written as $V_{h1} = V_{11} + V_{22} + V_{25} + V_{14}$. If we define a retina cycle as the time spent for the configuration of the coefficients kernel and the preprocessing of the image, the evaluation of the gradient on the vertical direction only spends a frame acquisition and two retina cycles. By generalization, the estimation of the complete gradient along the two axes spend 4 cycles because it involves 4 dynamic configurations.

In short, the dynamic assignment of coefficient values from the external processor gives the system some interesting dynamic properties. The system can be easily reconfigured by changing the internal coefficients for the masks between two successive computations. First, this allows the possibility to dynamically change the image processing algorithms embedded in the sensor. Secondly, this enables the evaluation of some complex pixel-level algorithms, implying different successive convolutions. The images can be captured at higher framerates than the standard framerate, processed by exploiting the the analog memories and the reconfigurable processing elements and output at a lower framerate depending of the number of the dynamic reconfigurations. Moreover, the analog arithmetic units implementing these pixel-level convolutions drastically decrease the number of single operations such as additions and multiplications executed by an external processor (an FPGA in our case) as shown in Figure 7. Indeed, in the case of our experimental 64 × 64 pixel sensor, the peak performance is equivalent to 4 parallel signed multiplications by pixel at 10 000 frames/s, that is, more than 160 million multiplications per second.

With a VGA resolution (640 × 480), the performance level would increase to a factor of 75, leading to about 12 billion multiplications per second. Processing this data flow by external processors will imply important hardware resources in order to cope with the temporal constraints.

As an illustration of the Sobel algorithm, Figure 12 is an example sequence of 16 images of a moving object, namely, an electric fan. Two white specific markers are placed on the fan, that is a small circle near the rotor and a painted blade. The speed rotation of the fan is 3750 rpm. In order to capture such a rapidly moving object, a short integration time (100 microseconds) was used for the frames acquisition. The Sobel algorithm allows to distinguish clearly the two white markers even with a high framerate.

### 6.3. Strategies used for general spatial filter

In the preceding sections, we focused on $2 \times 2$ and $3 \times 3$ convolution masks. In the case of a $2 \times 2$ mask, the coefficients are fixed once before the beginning of the acquisition frame. In the case of a $3 \times 3$ mask, two possibilities can occur. First, the $3 \times 3$ mask presents some symmetrical properties (such as the Sobel kernel) and then the coefficients values can be fixed as in a $2 \times 2$ mask. Second, if the mask is not symmetric, it is necessary to dynamically reconfigure the coefficients during the acquisition frame. For masks which size is greater than $3 \times 3$ and more generally in the case of an $N \times N$ mask, a dynamic reconfiguration of coefficients is necessary during the acquisition frame in order to evaluate the successive values of the linear combinations of pixels.

### 7. COMPARISON WITH OTHER SIMD VISION CHIPS

Table 2 shows an overview of some representative SIMD vision chips based on different alternatives for implementing...
vision processing at focal plane. The first column corresponds to the chip described in this paper. On the second column, we can find the main characteristics of SCAMP-3, a general purpose processor array implementing a variety of low-level image processing tasks at a high framerate. The third column describes a multiple instruction multiple data processing chip (MIMD IP Chip) performing spatial convolutions using kernels from $3 \times 3$ to $11 \times 11$. The fourth column presents a vision chip integrating an imager and an array of mixed-signal SIMD processing elements that can process gray scale images with cellular neural network universal machines (CNN-UMs) mode of operation. The fifth vision chip in the table is a programmable SIMD vision chip that can perform various early visual processing such as edge detection, smoothing or filtering by chaining processing elements and reconfiguring the hardware dynamically. Finally, the last one is a programmable artificial retina in which each pixel contains a tiny digital processing element capable of gray-level image processing from low- to mid-level vision (motion detection, segmentation, pattern recognition).

Compared to this state-of-the-art of high-speed CMOS image sensors, one easily sees that the chip reported in this paper leads to some major improvements. With a pixel size of $35 \mu m \times 35 \mu m$, the pixel pitch is almost 1.5 more compact than the smallest pixel described in [44, 45]. This contributes either to a better resolution of the sensor for a given chip area or a lower cost for a given resolution. At the same time, as compared with the other processing elements, our solution relies on a compact analog arithmetic unit (A2U) implemented at pixel-level. With basic image processing, the maximal framerate slows down to about 5 000 fps. The potential for dynamic reconfiguration of the sensor was also demonstrated in the case of the Sobel operator.

The next step in our research will be the design of a similar circuit in a modern 130 nm CMOS technology. The main objective will be to design a pixel of less than $10 \mu m \times 10 \mu m$ pixel contains 38 transistors implementing a circuit with photocurrent integration, two analog memory, amplifier, and multiplexer ([AM]^2), and an analog arithmetic unit (A2U).

Experimental chip results reveal that raw image acquisition at 10 000 frames per second can be easily achieved using the parallel A2U implemented at pixel-level. With basic image processing, the maximal framerate slows down to about 5 000 fps. The potential for dynamic reconfiguration of the sensor was also demonstrated in the case of the Sobel operator.

### 8. CONCLUSION AND PERSPECTIVES

An experimental pixel sensor implemented in a standard digital CMOS $0.35 \mu m$ process has been described in this paper. Each $35 \mu m \times 35 \mu m$ pixel contains 38 transistors implementing a circuit with photocurrent integration, two analog memory, amplifier, and multiplexer ([AM]^2), and an analog arithmetic unit (A2U).

Analog and digital technologies, we could consider the implementation of more sophisticated image processing operators dedicated to face localization and recognition. Previous work of our team [51] has demonstrated the needs of dedicated CMOS sensors embedding low-level image processing such as features extraction. Moreover, actual works [52] focus on a recent face detector named convolutional face finder (CFF) [53]. CFF
is based on a multilayer convolutional neural architecture. The CFF consists of six successive neural layers. The first four layers extract characteristic features, and the last two perform the classification. Our objective would be to implement at pixel-level the first layers based on convolutions by different masks from 2 × 2 to 5 × 5.

In order to evaluate this future chip in some realistic conditions, we would like to design a CIF sensor (352 × 288 pixels), which leads to a 3.2 mm × 2.4 mm in a 130 nm technology. The exploitation of high FPS capability with this sensor could be achieved by two complementary ways. The first one is to integrate a dedicated input/output module, which is able to cope with a Giga pixel per second bandwidth. Such modules have been already designed in other high-speed CMOS sensors. As an example, we can cite the digital pixel sensor [24] with its 64 bit (8-pixel) wide bus operating at 167 MHz, able to output 1.33 GB/s. The second way is to build a large sensor by assembling 64 × 64 pixel modules with a dedicated output bus for each of them. For example, with a 384 × 256 pixel sensor, this solution only requires 6 × 4 = 24 dedicated outputs. In the same time, we will focus on the development of a fast analog to digital converter (ADC). The integration of this ADC on future chips will allow us to provide new and sophisticated vision systems on chip (ViSOC) dedicated to digital embedded image processing at thousands of frames per second.

REFERENCES


Preliminary call for papers

The 2011 European Signal Processing Conference (EUSIPCO-2011) is the nineteenth in a series of conferences promoted by the European Association for Signal Processing (EURASIP, www.eurasip.org). This year edition will take place in Barcelona, capital city of Catalonia (Spain), and will be jointly organized by the Centre Tecnològic de Telecomunicacions de Catalunya (CTTC) and the Universitat Politècnica de Catalunya (UPC).

EUSIPCO-2011 will focus on key aspects of signal processing theory and applications as listed below. Acceptance of submissions will be based on quality, relevance and originality. Accepted papers will be published in the EUSIPCO proceedings and presented during the conference. Paper submissions, proposals for tutorials and proposals for special sessions are invited in, but not limited to, the following areas of interest.

Areas of Interest

- Audio and electro-acoustics.
- Design, implementation, and applications of signal processing systems.
- Multimedia signal processing and coding.
- Image and multidimensional signal processing.
- Signal detection and estimation.
- Sensor array and multi-channel signal processing.
- Sensor fusion in networked systems.
- Signal processing for communications.
- Medical imaging and image analysis.
- Non-stationary, non-linear and non-Gaussian signal processing.

Submissions

 Procedures to submit a paper and proposals for special sessions and tutorials will be detailed at www.eusipco2011.org. Submitted papers must be camera-ready, no more than 5 pages long, and conforming to the standard specified on the EUSIPCO 2011 web site. First authors who are registered students can participate in the best student paper competition.

Important Deadlines:

<table>
<thead>
<tr>
<th>Event</th>
<th>Deadline</th>
</tr>
</thead>
<tbody>
<tr>
<td>Proposals for special sessions</td>
<td>15 Dec 2010</td>
</tr>
<tr>
<td>Proposals for tutorials</td>
<td>18 Feb 2011</td>
</tr>
<tr>
<td>Electronic submission of full papers</td>
<td>21 Feb 2011</td>
</tr>
<tr>
<td>Notification of acceptance</td>
<td>23 May 2011</td>
</tr>
<tr>
<td>Submission of camera-ready papers</td>
<td>6 Jun 2011</td>
</tr>
</tbody>
</table>

Webpage: www.eusipco2011.org