

A 8 bits Pipeline Analog to Digital Converter Design for High Speed Camera Application

Eri Prasetyo, Hamzah Afandi, Nurul Huda)*
Dominique Ginhac , Michel Paindavoine)**

**Center for Microelectronics & Images Processing
Gundarama university , Indonesia*

***Laboratoire LE2I - UMR CNRS 5158
Université de Bourgogne
21078 Dijon Cedex – FRANCE*

*E-mail: (dginhac,paindav)@u-bourgogne.fr
(eri, huda,hamzah)@staff.gunadarma.ac.id*

Abstract - This paper describes a pipeline analog-to-digital converter is implemented for high speed camera. In the pipeline ADC design, prime factor is designing operational amplifier with high gain so ADC have been high speed. The other advantage of pipeline is simple on concept, easy to implement in layout and have flexibility to increase speed. We made design and simulation using Mentor Graphics Software with 0.6 μm CMOS technology with a total power dissipation of 75.47 mW. Circuit techniques used include a precise comparator, operational amplifier and clock management. A switched capacitor is used to sample and multiplying at each stage. Simulation a worst case DNL and INL of 0.75 LSB. The design operates at 5 V dc.

The ADC achieves a SNDR of 44.86 dB.

keywords: pipeline, switched capacitor, clock management

A 8 bits Pipeline Analog to Digital Converter Design for High Speed Camera Application

Abstract - This paper describes a pipeline analog-to-digital converter is implemented for high speed camera. In the pipeline ADC design, prime factor is designing operational amplifier with high gain so ADC have been high speed. The other advantage of pipeline is simple on concept, easy to implement in layout and have flexibility to increase speed. We made design and simulation using Mentor Graphics Software with 0.6 μm CMOS technology with a total power dissipation of 75.47 mW. Circuit techniques used include a precise comparator, operational amplifier and clock management. A switched capacitor is used to sample and multiplying at each stage. Simulation a worst case DNL and INL of 0.75 LSB. The design operates at 5 V dc. The ADC achieves a SNDR of 44.86 dB.

Keywords: pipeline, switched capacitor, clock management

1. Introduction

CMOS image sensors have evolved in the past years as a promising alternative to the conventional Charge Coupled device (CCD) technology. CMOS offer lower power consumption, more functionality and the possibility to integrate a complete camera system on one CHIP.

The high speed camera used matrices photodiode to capture objects and each photodiode send an analog pixel to matrices column. Output analog pixel is converted to digital pixel by ADC then output from ADC is processed by digital processor element. ADC is used to converter is pipeline. Diagram block high speed camera is shown in figure 1.

In the real time images processing, sensors function is important because it has function as transducer, so images can be processed to application for examples, face tracking and face recognition, medical imaging, industrial, sports and so on[4,5].

Figure 1. Describes 64x64 active pixel sensors (APS) is used capture object. We used the row decoder is charged to send to each line of pixels the control signals. The automatic scan of the whole array of pixels or sub windows of pixels is implemented by a sequential control unit which generates the internal signals to row and column decoders.

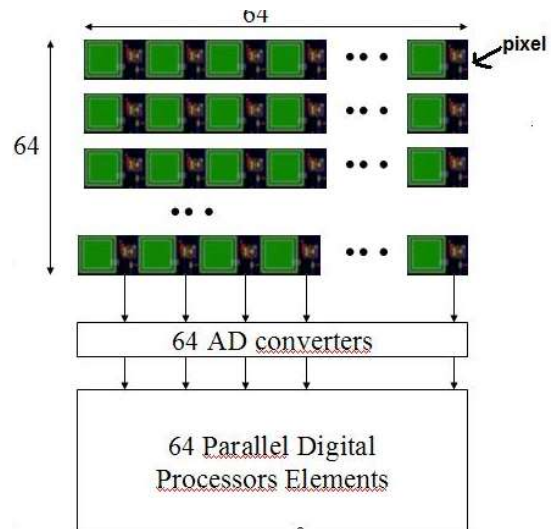


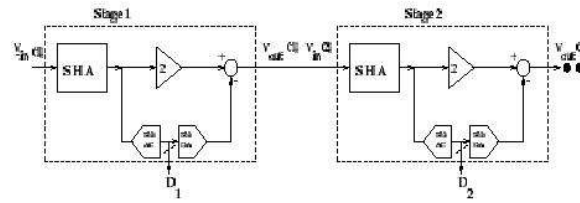
Figure 1. Diagram Block high speed camera

Number of ADC is used in the system are 64 on parallel condition. Function of ADC in the process is important to convert from analog pixels to digital pixels where output from APS is nearly 4K pixel with each pixel < 100 ns or same as 400 μs per images or 2500 images/s. so wherever we must design pipeline ADC which have transfer rate 80 Msamples/s.

2. One-Bit Per Stage Pipeline Architecture

Figure 2. One bit/ stage architecture

Figure 2 shows block diagram of an ideal N-stage, 1-bit per stage pipelined A/D converter. Each stage contributes a single bit to digital output. The most significant bits are resolved by first stage in the pipeline. The result of stage is



passed on the next stage where the cycle is repeated. A pipeline stage is implemented by the conventional switched capacitor (SC), it is shown at figure 3[4].

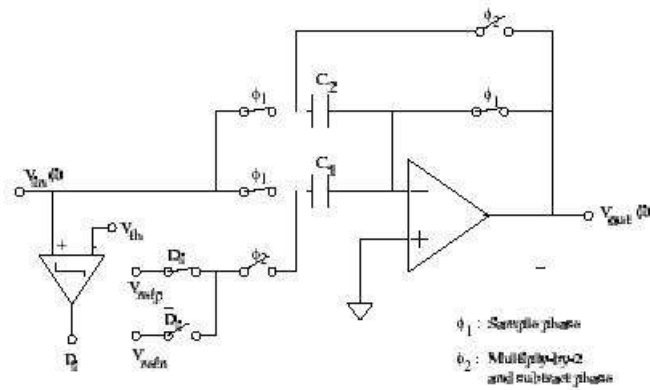


Figure 3. Scheme of switched capacitor pipelined A/D converter

V_{refp} is the positive reference voltage and V_{refn} is a negative reference voltage. Each stage consists of capacitor C_1 , C_2 , an operational amplifier and a comparator. Value of C_1 and C_2 are equal in my design. Each stage operates in two phases, a sampling phase and a multiplying phase.

During the sampling phase ϕ_1 , the comparator produces a digital output D_i . D_i is 1 if $V_{in} > V_{th}$ and D_i is 0 if $V_{in} < V_{th}$, where V_{th} is the threshold voltage defined midway between V_{refp} and V_{refn} . During multiplying phase, C_2 is connected to the output of the operational amplifier and C_1 is connected to either the reference voltage V_{refp} or V_{refn} , depending on the bit value D_i . If $D_i = 1$, C_1 is connected to V_{refp} , resulting in the resedu (V_{out}) is :

$$V_{out}(i) = 2 \times V_{in}(i) - D_i \cdot V_{refp} \quad (1)$$

Otherwise, C_1 is connected to V_{refn} , giving an output voltage :

$$V_{out}(i) = 2 \times V_{in}(i) - \bar{D}_i \cdot V_{refn} \quad (2)$$

3. Comparator

Precision comparator is implemented to

each stage of the ADC. We prefer to use precision comparator then digital correction to minimize offset error of comparator and better output of ADC.

This comparator consists of three blocks: preamplifier, decision circuit and output buffer. First block is the input preamplifier which the circuit is a differential amplifier with active loads. The size of transistors m_2 and m_3 are set by considering the diff-amp transconductance and the input capacitance. Second block is a positive feedback or decision circuit, it is the heart of the comparator. The circuit uses positive feedback from the cross gate connection of m_{11} and m_{12} to increase the gain of the decision element. Third stage is output buffer; it is to convert the output of the decision circuit into a logic signal. The inverter (m_{20} and m_{21}) is added to isolate any load capacitance from the self biasing differential amplifier. The complete circuit of comparator is shown in figure 4.

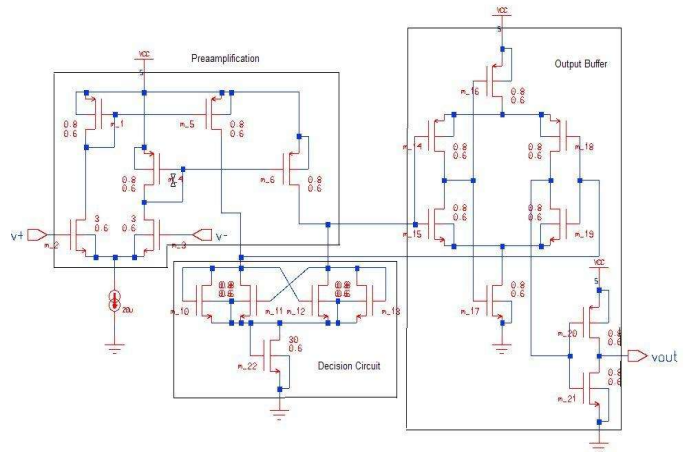


Figure 4. The comparator circuit

4. Operational Amplifier

In this pipeline ADCs, operational amplifier is very important to get accurately result. We used an operational transconductance amplifier which has a gain of approximately 55 dB for a bias current of 2.5 μ A with $V_{dd} = 5$ V and $V_{ss} = -5$ V. A value of loading capacitor is 0.1 Pf. The complete circuit is shown in figure 5. Transistors $m_{1_1_1}$ and m_{1_1} functions as a constant current source, and transistors m_1 , m_2

and m_3 functions as two current mirror 'pairs'. The transistors m_4, m_5, m_6 and m_7 are the differential amplifier.

Transistor m_9 is an output amplifier stage. In the simulation, we got the resultat for phase margin (PM) was -145 degree, A gain was 55 dB and Gain bandwidth product was 800 MHz. A power dissipation mesured of 10.825 mW.

5. Clock Management

In the design pipeline A/D converter use latch technique is used to hold active condition at multiplying ϕ_2 and non active condition at sampling ϕ_1 until next stage begin to execute sampling phase. This purpose to keep the output voltage of residu from before stage conformity at input next stage.

The clock management system use counter to count some clock to active the address decoder from each stage.

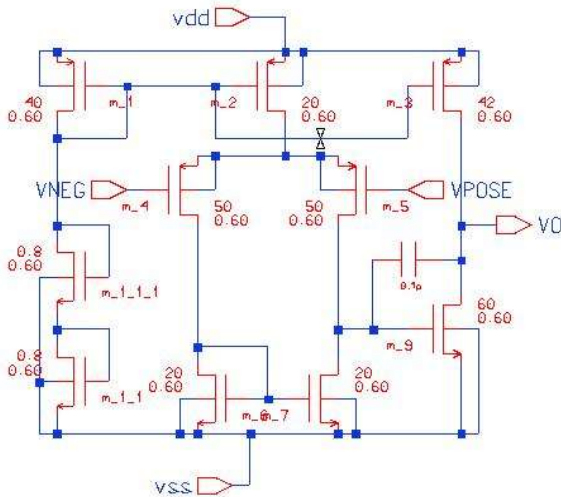


Figure 5. Transconductance OP-AMP

Signal output decoder active reset signal so the clock management begin working. This work is begun from early address to last address. Ending of address decoder, a stop decoder give reset signal Stopping activity pipeline ADC's. The complete circuit is shown at figure 6.

Figure 6. The circuit of clock management

6. Result

One stage A/D converter layout was estimated to occupy about $174 \mu\text{m} \times 89 \mu\text{m}$, it is seen at figure 7.

Figure 8 shows the dc linearity of the ADC at conversion rate of 20 Msamples/s. In the figure 8(a), the CODE is plotted versus integral nonlinearity (INL) value and figure 8(b), the CODE is plotted versus differential nonlinearity (DNL). Note that since each simulation lasted 20 minutes, only 25 codes were tested. As shown, the worst INL is less than 0.8 LSB; the DNL is less then 0.8 LSB.

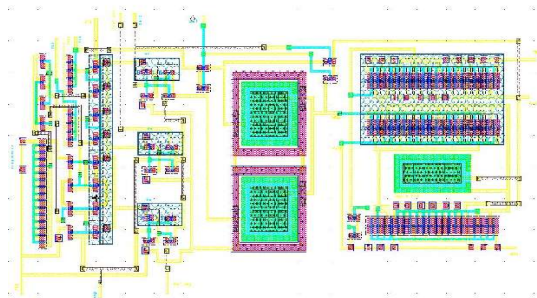


Figure 7. One stage A/D converter layout

Figure 9 shows the output of Fast Fourier transform (FFT) on a block of 1024 consecutive codes. The conversion rate is 20 Msamples/s, and the input is full scale sines wive at 10 MHz. From curve FFT, The signal-to-noise plus distortions ratio (SNDR) is obtained about 44.86 dB. The effective number of bits (ENOB) is calculated environ 7.2 bits.

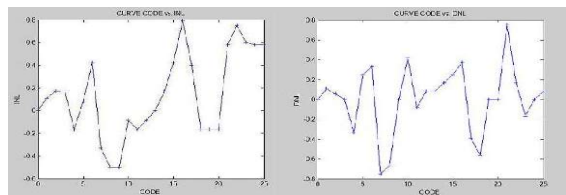


Figure 8. (a) Curve of Code vs INL and (b) Curve of Code vs DNL

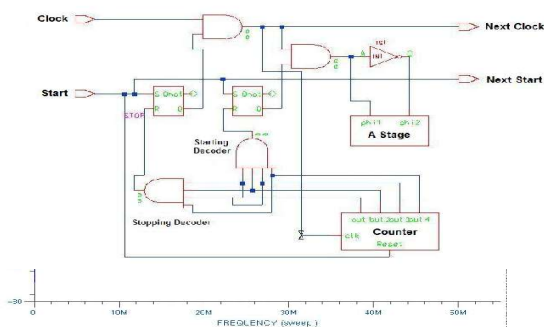


Figure 9. Curve of FFT

7. Conclusion

The pipeline ADC 8 bits, 80 Msamples/s were implemented in 0.6 μm technology with total power dissipation 75.47 mW. Refer to result of experiment; the ADC can be implemented for high speed camera.

The system use clock management to manage data conversion so that the system is Simple and have good precision.

References

- [1] Timothy M. Hancock, Scott M. Pernia, and Adam C. Zeeb, "A digitally corrected 1.5 bits/stage low power 80 Msamples/s 10-bits pipelined ADC", technical report, University of Michigan, December 2002.
- [2] Hao-Yu, xun-Gong, and Juo-Jung hung," A low power 10 bits 80 Msamples pipeline ADC", Technical report, ECCS department

University of Michigan tech., 2003.

- [3] S.H. Lewis, H. Scott Feterman, George F. Gross Jr., R. Ramachandran, and T.R. Vismanathan., "10-b 20 Msamples/s analog to digital converter", *Journal of IEEE solid state circuit*, 27:351-358, March 1992.
- [4] M. Paindavoine,"High-speed camera with embedded real time image processing", in seminar information technology of Gunadarma University, June 2006.
- [5] Eri Prasetyo, Dominique Ginhac and M. Paindavoine ,"principles of CMOS sensors dedicated to face tracking and recognition", *In CAMP05*, July 2005.
- [6] R. Samer and Jan Van der Spiegel and K. Nagaraj, "Background digital error correction technique for pipeline ADC, " *IEEE*, 2001.
- [7] A. Shabra and Hae-Seung Lee, " Over sampled pipelined A/D converter with mismatch shaping," *Journal of IEEE Solid State Circuit*, vol. 37, no. 5, May 2002
- [8] Dwight U. Thomson and Bruce A. Wooley, "A 15-b pipelined CMOS floating point A/D converter, " *Journal of IEEE Solid State Circuit*, vol. 36, no. 2, February 2001.