Principles of a CMOS sensor dedicated to face tracking and recognition

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***Abstract*— This paper describes the main principles of a vision sensor dedicated to the detecting and tracking faces in video sequences. For this purpose, a current mode CMOS active sensor has been designed using an array of pixels that are amplified by using current mirrors of column amplifier. This circuit is simulated using Mentor Graphics™software with parameters of a 0.6 μm CMOS process. The circuit design is added with a sequential control unit which purpose is to realise capture of subwindows at any location and any size in the whole image.**

keywords : ***CMOS active sensor, embedded system, real time image processing***

I. Introduction

A system capable of doing face localization and recognition in real time has many applications in intelligent man-machine interfaces and in other domains such as very low bandwidth video conferencing, and video e-mail.

This paper describes the main principles of a vision system, allowing to detect automatically the faces presence, to localize and to follow them in video sequences. Some preliminary works have shown that simplified RBF networks gave interesting results[1][2] but imposed a fast feature extraction to reduce the size of the input vectors of the RBF network. So, the main goal of the current project is the development and the characterisation of a specific CMOS sensor. A very large scale integration retina is proposed to realize the image acquisition, to extract a window of interest in the whole image and to evaluate means values of consecutive pixels on lines and columns.

A first image sensor with electronic shutter has been integrated in a 0.6 μm digital CMOS technology. The pixel cell consists of four transistors and a photodiode. Each pixel measures 30 μm by 30 μm and has a fill factor of about 40%. Each selected pixel produces a current which is transfered to the column readout amplifiers and converted by a pipeline ADC to produce a digital output. The two analog and digital values are then multiplexed to the output of the sensor.

This retina also includes a logic command in order to realize acquisition of subwindows with random size and position.

Actual and future work will focus on the development of the feature extracting architecture dedicated to the mean evaluation of consecutive pixel which will be used as input vectors of the RBF network and a pipeline analog to digital converter.

II. Active Pixel Sensor

An active pixel sensor (APS) is defined as a detector array that has at least one active transistor within the pixel unit cell[3]. Currently, active pixel sensor technology integrates electronic signal processing and control with smart camera function onto the same single chip as a high performance image sensor[4]. CMOS image sensors with integrated signal processing have been implemented for a number of applications[5]. Most current CMOS imaging arrays have been designed for video applications, and digital photography. Improvement continues to be made in the growing digital image. A current mode image sensor has several advantages for example, low power supply, smaller place, higher operation speed[6], [7], [8].

The following sections of this paper describe the design of the image sensor using a standard 0.6 μm CMOS process. The design is based on the integration of four MOS transistors for each pixel, a column readout amplifier, a sequential control unit which includes variable input counters, decoders, multiplexers and finaly an analog to digital converter. Results based on design and simulation with Mentor Graphics™software are presented for each part of the circuit.

III. System Architecture

The architecture of the proposed image sensor is shown in figure 1.

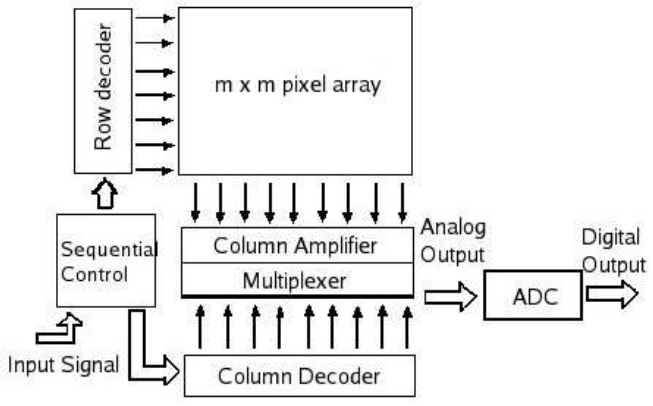

Fig. 1. Image sensor system architecture

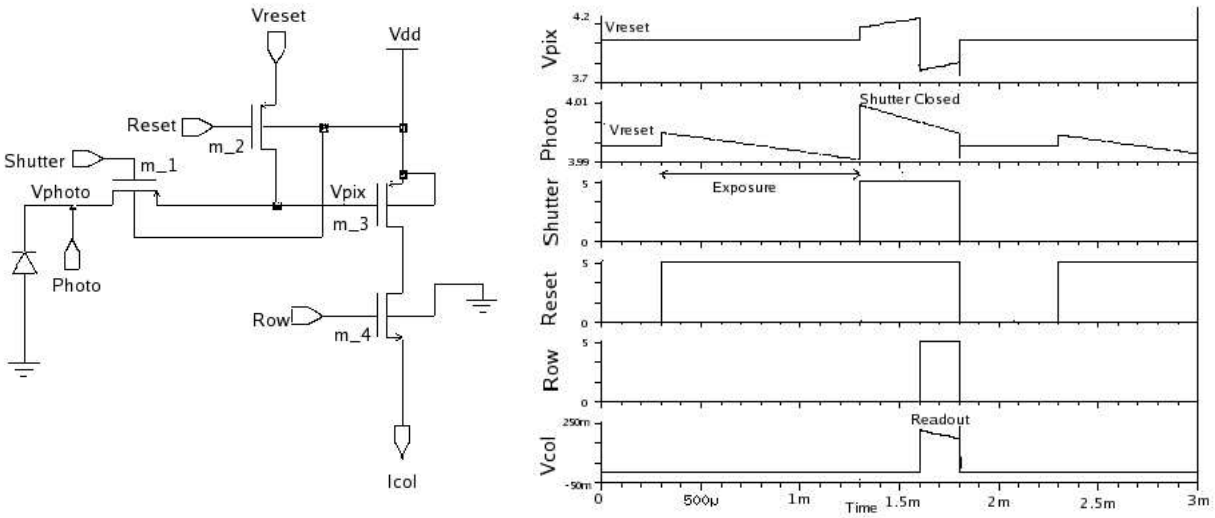

Fig. 2. Pixel circuit schematic and results of simulation

This figure first describes the core of the system represented by the m x m array of transistors active pixels. On the left, the second block, the row decoder is charged to send to each line of pixels the control signals allowing pixel resetting, shutter opening or closing, pixel readout, ... On the botton of the circuit, the third block is made up of amplifiers, multiplexers and column decoders whose purpose is to detect, amplify and route the signal resulting from readout column to the output of the circuit. The automatic scan of the whole array of pixels or a subwindow of pixels is implemented by a sequential control unit which generates the internal signals to the row and column decoders. Finaly, the analogic output voltages are proportional to the gray scale intensity of the image. They are passed to an analog to digital converter (ADC) (as seen on the right of the block diagram). This ADC allows the conversion of analogic values in digitals value which will be later processed by a DSP or a FPGA outside the acquisition system.

IV. Design of the Active Pixel System

We used a standard pixel as described in the left part of figure 2 because it is a simple and stable design[9][5][10]. It consists of 3 PMOS transistors, a NMOS transistor for row access and a photodiode. *m_1* is the shutter transistor, *m_2* is the reset transistor, the transistor *m_3* acts as a transconductance buffer that converts the voltage at V_{pix} into a current. The vertical column lines in the array are implemented using second-layer metal. First layer metal is used for the horizontal row lines. Third-layer metal is connected to V_{ss} and covers all active areas of the pixel except the photodiodes.

Prior to the image acquisition, *m1* and *m_2* are on, resetting node V_{photo} and V_{pix} to the V_{reset} value. After reset, when *m_1* is on and *m_2* turned off, the charges generated by absorption of light are integrated onto the parasitic capacitances of the photodiode and the transistor *m_3*. So, during the exposure period, voltage is accumulated at node V_{photo} and V_{pix}. At the end of the exposure period, the shutter is closed by turning off *m_1*. Consequently, the photosignal is stored as a voltage on node V_{pix}. Finaly, during readout, the row access transistor *m_4* is turned on, and the drain current of *m_3* is fed via the column line to the column readout amplifier.

The right part of figure 2 shows the main waveforms (V_{Pix}, V_{Photo}, $V_{Shutter}$,V_{Reset},V_{Row} and V_{Col}) obtained during the simulation of one pixel. The pixels in a row are reseted by holding both reset and shutter low, turning on *m_1* and *m_2*. The voltages at nodes V_{photo} and V_{pix} are thereby reseted close to V_{reset}.

During exposure, reset goes high (*m_2* turns off) while shutter is unchanged at a low value (*m_1* remains on). So, the photocurrent can be integrated onto the parasitic capacitances at V_{photo} and V_{pix}. At the end of the exposure period, shutter is closed by turning off *m_1* and it is cutting off the photocurrent into the node V_{pix}. I_{col} can be read on the column bus when *m_4* is turned on (row is high). The voltage at the drain of *m_3* falls from V_{dd} to the bias voltage of the column line, and this change couples a small negative offset into node V_{pix}. The drain current of *m_3* is fed via the column line to the column readout amplifier.

V. Design of the Column Amplifier

The figure 3 represents the electronic schematic of the column amplifier. The design of this amplifier provides a low impedance for the column lines, converts the readout current from the selected pixel into a voltage that is proportional to the integrated photovoltage in the pixel.

The concept of using current mirror amplifier column is to amplify signal by duplication at the column level. Amplification is achieved by designing a current mirror m_{20} and m_{24} with ratio $W/L_{m_{20}} = n \times W/L_{m_{24}}$.

The transistors m_{22} and m_{23} are added to enhance the output impedance of the current mirror. The circuit inclu-

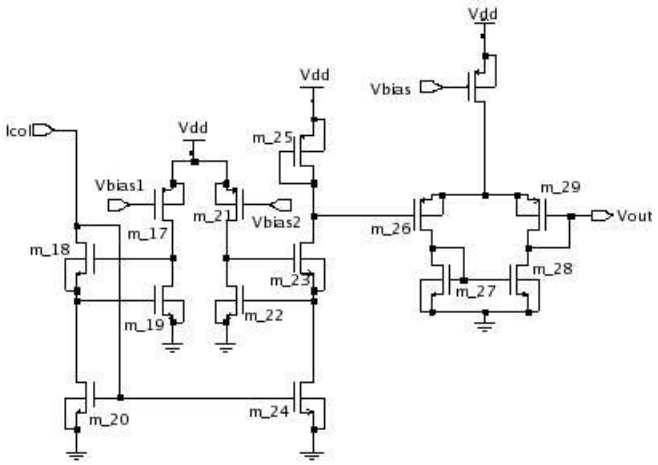

Fig. 3. Column amplifier schematic

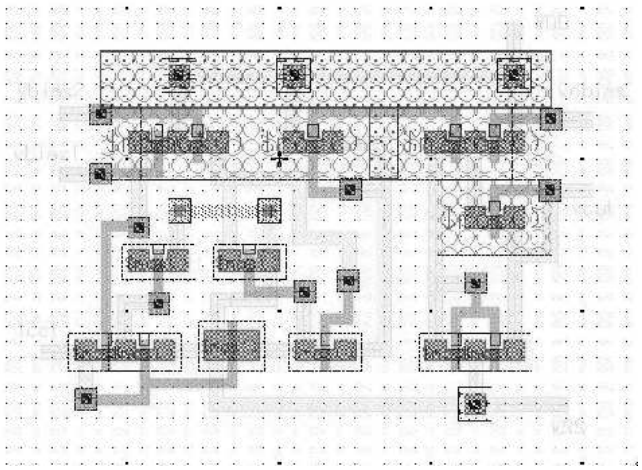

Fig. 5. Layout of the column amplifier

ding m_{17}, m_{18}, m_{20} operates almost identically to a diode-connected transistor, it is used to ensure that all the transistors bias voltages are matched to the output side (m_{22}, m_{23}, m_{24}). The transistors m_{17}, m_{21} are used to bias the feedback circuit. The transistors m_{26}, m_{27}, m_{28}, m_{29}, m_{30} make up a differential unity gain amplifier. Once the current signal has been amplified by column current miroir amplifier, its output is suitable for any subsequent current mode image processing, either in continuous time or integration mode. In our case, these outputs will be used as inputs for the feature extracting architecture dedicated to the mean evaluation of consecutive pixels.

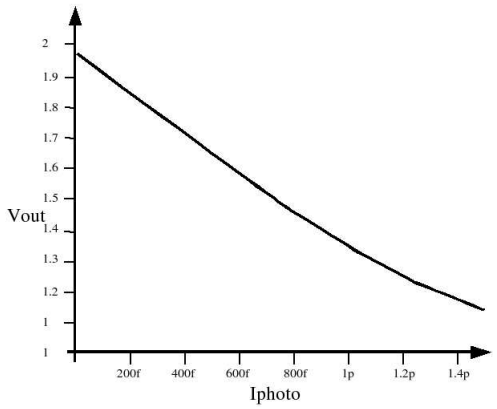

Fig. 4. Simulated voltage output of the column amplifier

The pixel with its column amplifier has been simulated for a large range of photodiode currents as seen on figure 4. The output voltages are plotted as a function of input photocurrents. Good output linearity is observed, even at very low photocurrent.

The figure 5 represents the layout of the column amplifier

VI. Design of the Sequential Control Unit

A framework dedicated to the sequential readout of successive rows and columns has been designed. The system offers the availability to program the location and the size of any window of interest in the whole image. Advantages of a such technology are large : random access of any pixel or subwindow, increase of acquisition frequency, ... In our main goal of face tracking, these aspects are crucial because only windows of interest will be scanned by the sensor, as illustrated in figure 6. This figure shows an acquisition of a subwindow of 4×4 pixels starting at the row 3 and column 4.

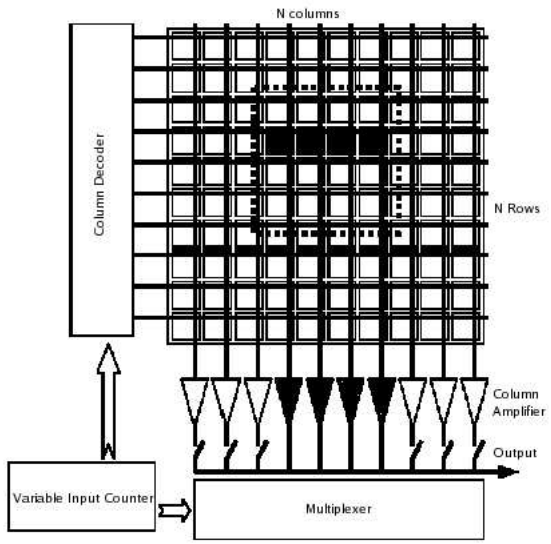

Fig. 6. Readout of a window of interest

Each line of pixels follows the same sequence of reading but at different moments in order to multiplex the outputs. As seen in section IV, each pixel is controlled by 3 signals : reset signal, shutter signal and select signal. The figure 7 shows the

readout sequence of 2 successive rows.

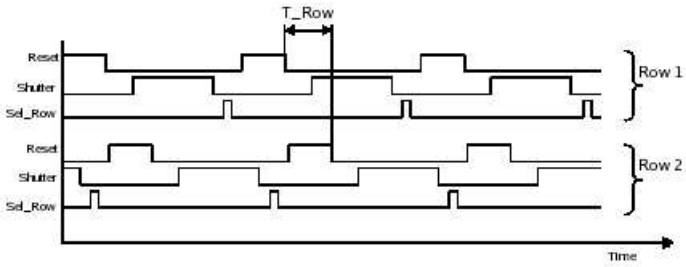

Fig. 7. Timing diagram of the rows control signals

To implement the sequential control, we need counters with variable inputs : the first for the starting position of the subwindow and the second for its ending position. Our design is inspired by a 74HC163 counter from Philips Semiconductors[11]. This circuit starts counting from a value which can be freely selected. It has been modified in order to add the second input corresponding to the stop value of the counting process. An example of a 4 bits counter can be seen on the figure 8.

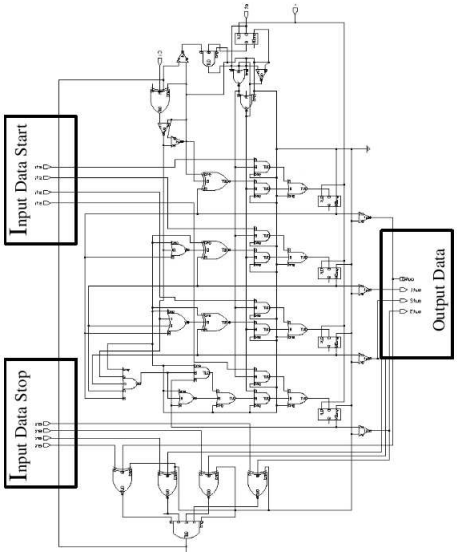

Fig. 8. A 4 bit counter circuit

The figure 9 describes the layout of a such counter. It measures 250 μm x 100 μm.

Associated with the counters, the control unit uses row decoders to active the pixels rows. The row decoder is adopted from [12]. A long L MOS transistor is used to pull low the output of the decoder when that particular output is not selected. The result is that all decoder outputs are zero except for the output that is selected by the input address. Two inverters are used to drive the word line capacitance.

Finaly, a multiplexer is used to select and pass output voltages from the column amplifiers. We use a simple design based on pairs of transistors Nmos and Pmos.

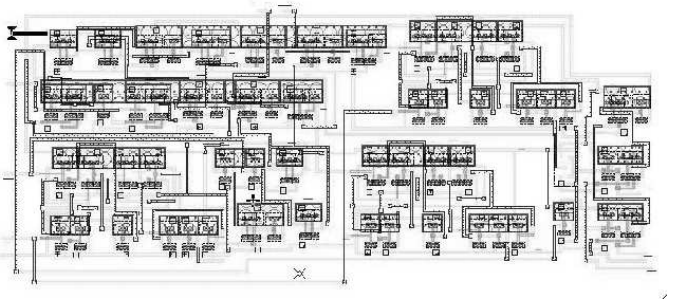

Fig. 9. Layout of a 4 bit counter

VII. Design of the Analog To Digital Converter

Most designs of video-rate analog to digital converters (ADC's) of 8 bit resolution are implemented through flash architectures and bipolar technologies[13]. In recent years, pipelined switched capacitor topologies have emerged as an approach to implement power efficient nyquist-rate ADCs that have medium-to-high resolution (10-13 bits) at medium-to-high conversion rates[14].

This paper presents a 8 bit ADC operating at a 5 V supply that achieves a sample rate of about 20 Msamples/s. An experimental prototype of this converter has been implemented in 0.6 μm.

A. One-Bit Per Stage Pipeline Architecture

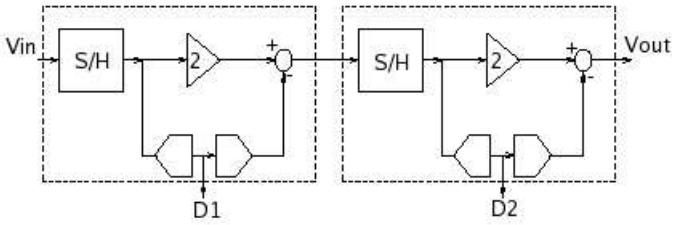

Fig. 10. One bit per stage architecture

Figure 10 shows the block diagram of a 1-bit per stage pipelined A/D converter. The pipelined ADC consists of N stages connected in series, two stages are only shown on the figure 10. Each stage contains a sample and hold (S/H), a comparator, a subtractor and an amplifier with a gain of two. The pipelined ADC is an N-step converter, with 1 bit being converted per stage. The most significant bits are resolved by the first stages in the pipeline. The result of each stage is passed to the next stage in which the cycle is repeated. A pipeline stage is implemented by the conventional switched capacitor[15] as shown in the figure 11.

Each stage consists of two capacitors C_1 and C_2 for which the values are nominally identical, an operational amplifier and a comparator. Each stage operates in two phases : a sampling phase and a multiplying phase.

During the sampling phase ϕ_1, the comparator produces a digital output D_i. D_i is 1 if $V_{in} > V_{th}$ and D_i is 0 if $V_{in} < V_{th}$,

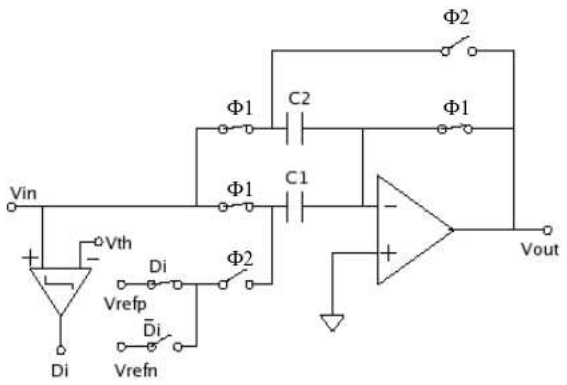

Fig. 11. The switched capacitor pipelined A/D converter

where V_{th} is the threshold voltage defined as the mean value between V_{refp} and V_{refn}. V_{refp} is defined as the positive reference voltage and V_{refn} as a negative reference voltage.

During the multiplying phase, C_2 is connected to the output of the operational amplifier and C_1 is connected to either the reference voltage V_{refp} or V_{refn}, depending on the bit value D_i. If $D_i = 1$, C_1 is connected to V_{refp}, resulting in the following remainder (V_{out}) :

$$V_{out}(i) = 2\ V_{in}(i) - D_i V_{refp}$$

Otherwise, C1 is connected to V_{refn}, giving an output voltage :

$$V_{out}(i) = 2V_{in}(i) - \overline{D}_i V_{refn}$$

B. Operational amplifier

In this pipeline ADCs, the operational amplifier is very important to get results with a good accuracy.

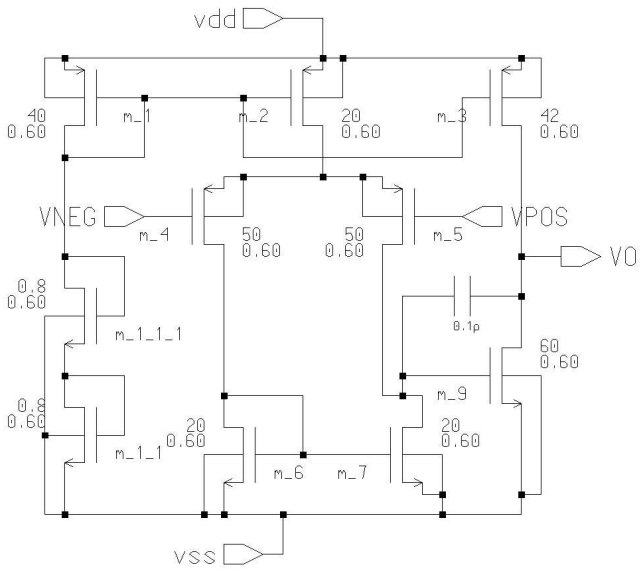

Fig. 12. Transconductance OP-AMP

We use an operational transconductance amplifier which has a gain of approximately 52 dB for a bias current of 2.5 μA with $V_{dd} = 5V$ and $V_{ss} = -5V$. The value of the load capacitor is 0.1 Pf.

The complete implementation is shown in figure 12. Transistors m_1_1_1 and m_1_1 are used as a constant current source, and transistors m_1, m_2 and m_3 work as two current mirror pairs. The transistors m_4, m_5, m_6 and m_7 are the differential amplifier. Transistor m_9 is an output amplifier stage.

One stage A/D converter layout was estimated to occupy about 174 μm x 89 μm, it is seen at figure 13.

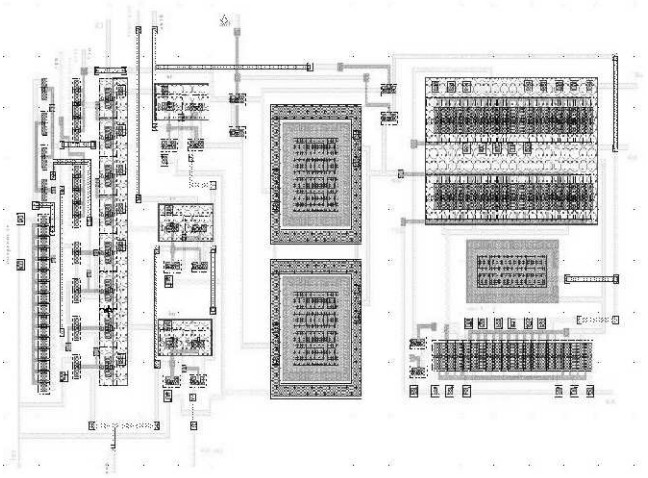

Fig. 13. One stage A/D converter layout

The simulation of one stage A/D converter can be seen on the figure 14 on which the computed bit, the remainder, the input value and the clock are presented from top to bottom. The input value is $V_{in} = 3V$ involving the output bit D_i obtains a high value. The remainder is then evaluated as the difference between $2V_{in}$ and V_{refp} (ie $2 * 3 - 5 = 1V$).

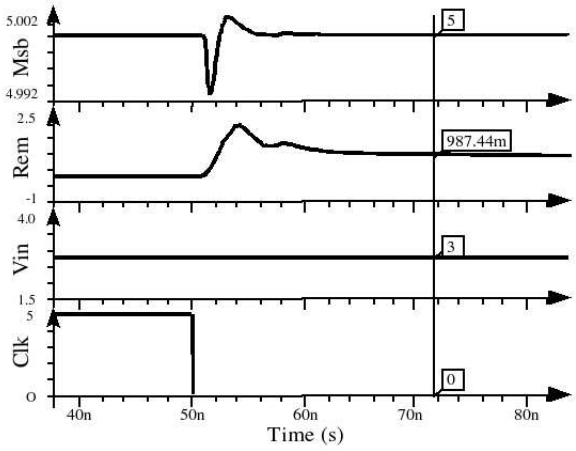

Fig. 14. Simulation of one stage A/D converter

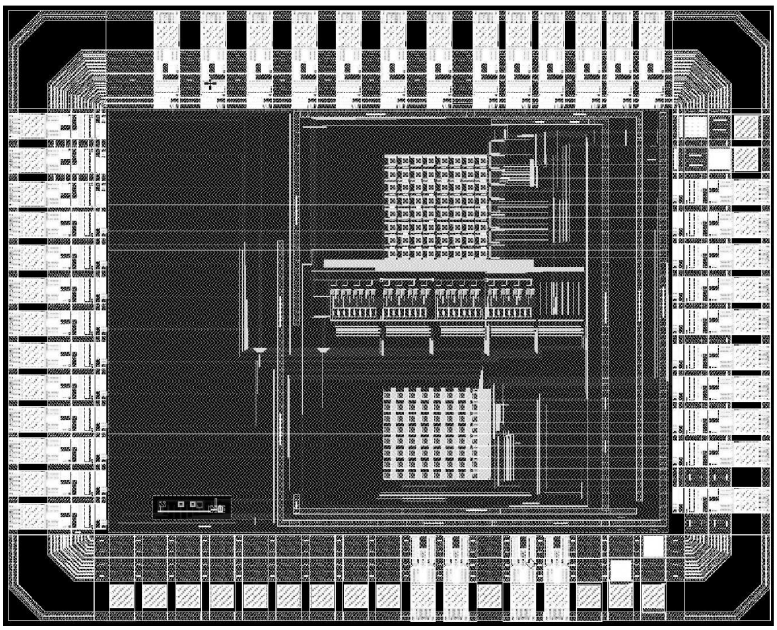

Fig. 15. Layout of the first circuit

VIII. Preliminary results

We have presented here results from simulations intended to evaluate and validate the efficiency of our approach. Every element described in this paper has been designed on a standard 0.6 μm CMOS Process. A first test circuit has been sent in foundry in october 2004 to be fabricated (see figure 15). This circuit will be available in the beginning of the next year and so, experimental results are expected in a near future.

IX. Conclusion

The design of a current mode CMOS active pixel image sensor with mode integration is presented in this paper. The circuit can work very well at small photocurrent. The circuit has been designed and simulated on a standard 0.6 μm CMOS process.

Actual work focuses on the last part of the sensor ie the development of the feature extracting architecture dedicated to the mean evaluation of consecutive pixels.

The next effort will be the fabrication of the real chip on a standard 0.6 μm or 0.35 μm CMOS process. Evaluation and comparaison of fabricated chip will be conducted refer to theoretical and simulated results.

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