High performance silicon imaging

Chapter 6: Smart cameras on a chip: using complementary metal oxide semiconductor (CMOS) image sensors to create smart vision chips

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Abstract:

Today, improvements in the growing digital imaging world continue to be made with two main image sensor technologies: charge coupled devices (CCD) and CMOS sensors. The continuous advances in CMOS technology for processors and memories have made CMOS sensor arrays a viable alternative to the popular CCD sensors. This led to the adoption of CMOS image sensors in several high-volume products, such as webcams, mobile phones, PDAs for example. New technologies provide the potential for integrating a significant amount of VLSI electronics into a single chip, greatly reducing the cost, power consumption, and size of the camera. By exploiting these advantages, innovative CMOS sensors have been developed. Moreover, the main advantage of CMOS image sensors is the flexibility to integrate signal processing at focal plane down to the pixel level. As CMOS image sensors technologies scale to 0.13 µm processes and under, processing units can be realized at chip level (system-on-chip approach), at column level by dedicating processing elements to one or more columns, or at pixel-level by integrating a specific processing unit in each pixel. By exploiting the ability to integrate sensing with analog or digital processing, new types of CMOS imaging systems can be designed for machine vision, surveillance, medical imaging, motion capture, pattern recognition among other applications.

Historically, most of the researches have focused on chip and column-level processing. Indeed, pixel-level processing is generally dismissed because pixel sizes are often too large to be of practical use. However, as CMOS scales, integrating a processing element at each pixel or group of neighboring pixels becomes feasible. This offers the opportunity to increase quality of imaging in terms of resolution or noise for example by integrating specific processing functions such as correlated double sampling, anti blooming, high dynamic range, and even all basic camera functions (color processing functions, color correction, white balance adjustment, gamma correction) onto the same camera-on-chip. Furthermore, employing a processing element per pixel offers the opportunity to achieve massively parallel computations and thus the ability to exploit the high-speed imaging capability of CMOS image sensors. As integrated circuits keep scaling down following Moore's Law, recent trends show a significant number of papers discussing the design of digital imaging systems that take advantage of the increasing number of available transistors integrated in each pixel in order to perform analog to digital conversion, data storage and sophisticated digital imaging processing.

In this book chapter, we first survey existing works on chip-level image processing applications embedded in high-performance CMOS imaging devices. However, simply integrating analog or digital blocks operating on the pixel flow does not fully exploit the potential of CMOS imaging technologies. So, in the remainder of this chapter, we focus on column-level and on chip-level image processing in which we can benefit from massively parallel computations to integrate complex image processing applications. Finally, we survey recent trends on three-dimensional integrated imagers. 3D stacking technology becomes an emerging solution to design powerful imaging systems because the sensor, the analog-to-digital converters and the image processors can be designed and optimized in different technologies, improving the global system performance.